

SYSTEM CO-SIMULATION OF RADIO DIGITAL FRONT END

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PRESENTATION PLAN

- 0 – SLD – System verification of digital radio front-end for base-band system
- 1 - CO-SIMULATION needs
- 2 - Existing ADS tool
- 3 - Advantages and drawbacks according to the needs
- 4 - Action plan, suggestions, open questions



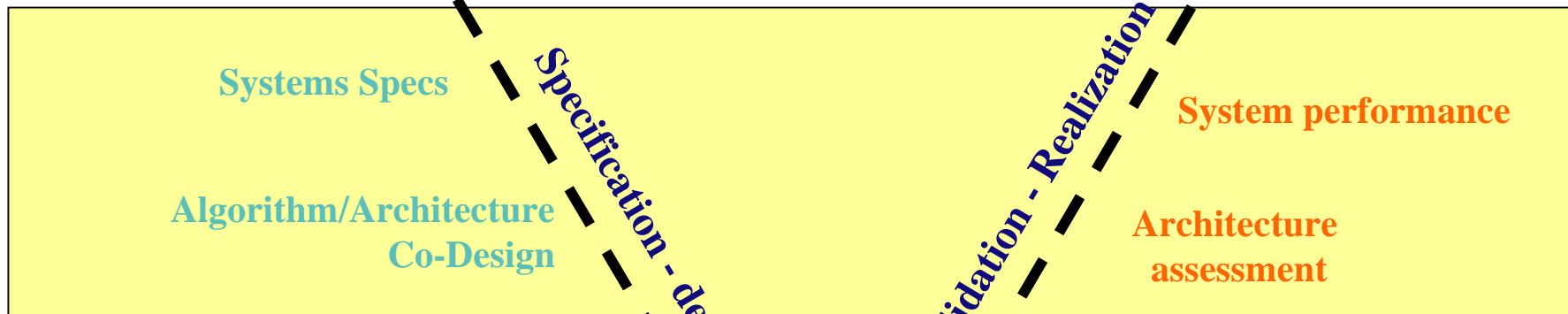
Position in System Level Design

Top-Down

Motivation for a RF Digital Transceiver
CO-SIMULATION



System Requirements



HW/SW codesign and communication layers

Integration/Generation of RTOS and Design Composition

Functional breakdown

Functional assembling

Modular design

Bottom-up



Fleur - A504
Specac - A508

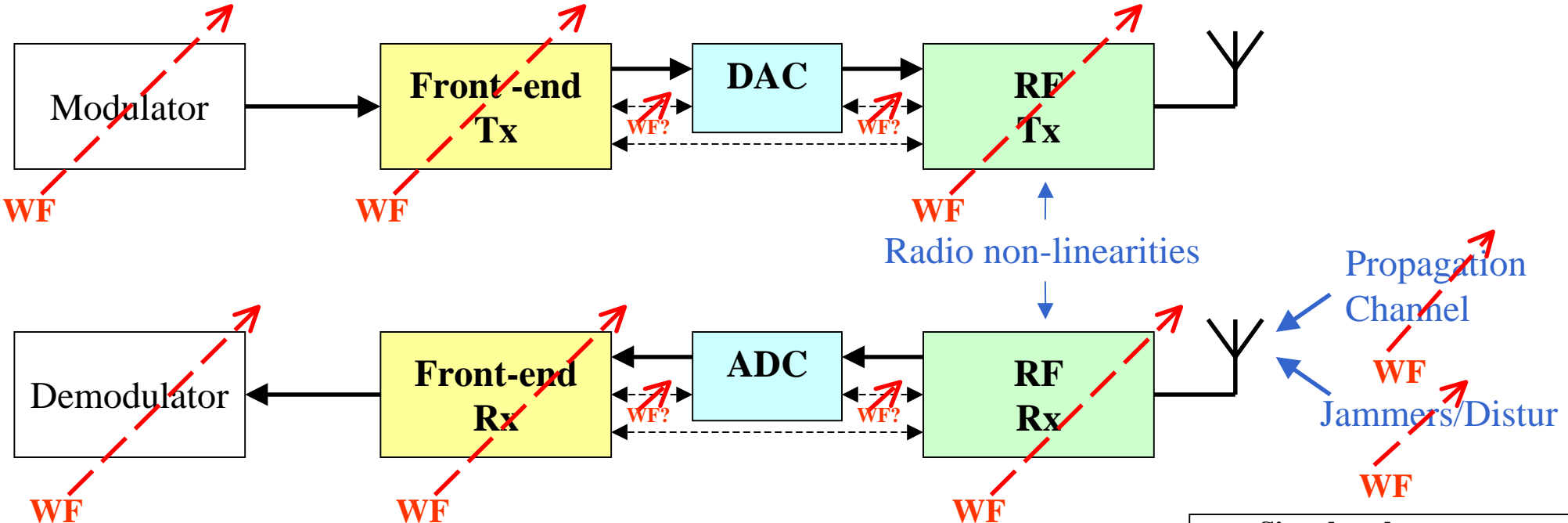
1 - CO-SIMULATION needs

**Digital Transceiver / RF Module
Wide band Transceiver**

=> DTX-RF Co-simulation and Co-verification



RCV & XMIT CHAINS TO SIMULATE



	Signal path
	Control
	Wave Form dependant

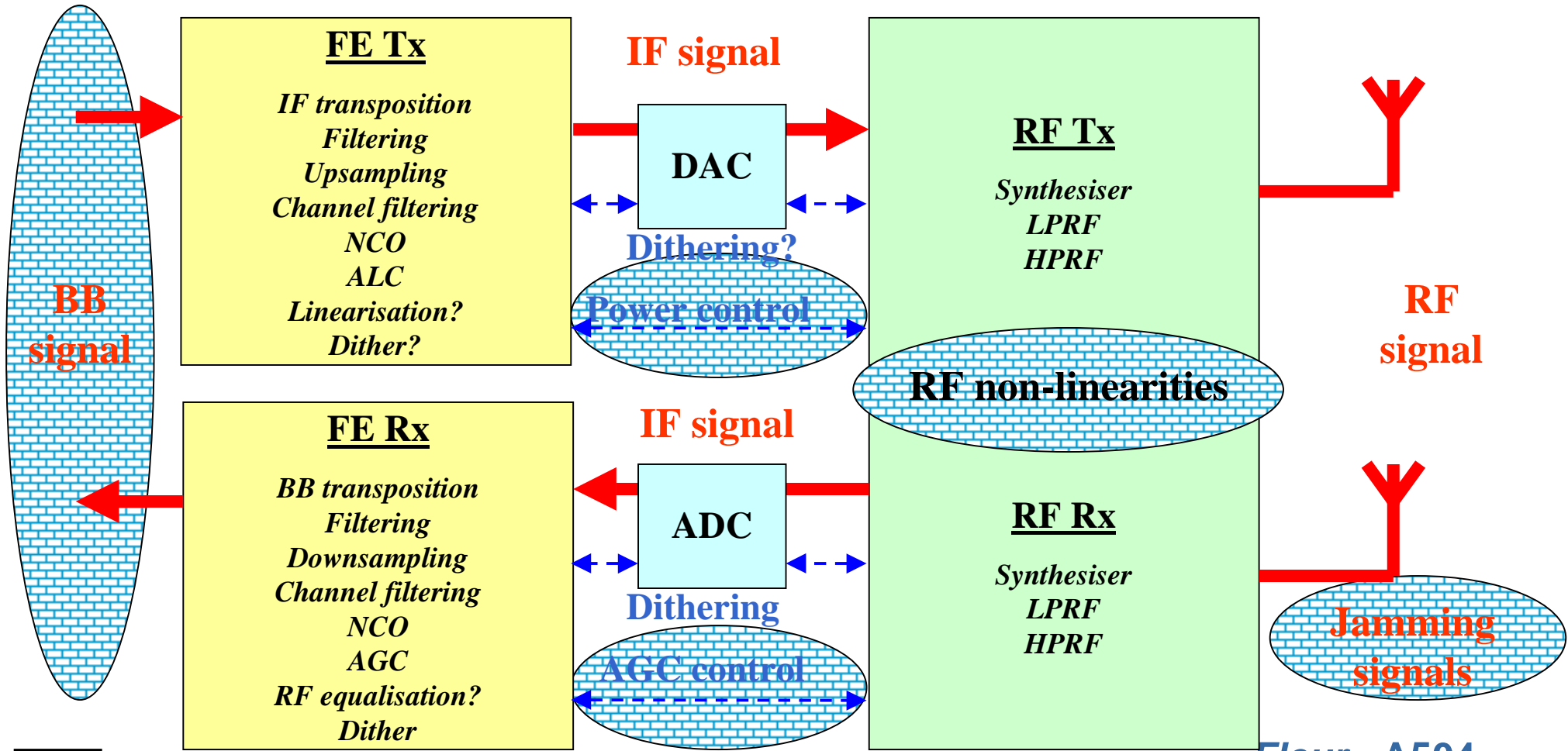
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FEATURES TO ANALYZE

Front End RF PART

 Issues tackled on ADS



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SYSTEM SIMULATION NEEDS AT SYSTEM LEVEL

❑ Simulation of feedback loops

- Rx : AGC
- Tx : Power Control (ALC)

❑ Simulation of the whole radio chain

- Rx, Tx
- Tx + Propagation channel + Rx → BER (if necessary)

❑ Simulation in a jammer context

❑ Simulation including the RF non-linearities



2 - ADS tools



ADS TOOLS FOR CO-SIMULATION

- ❑ **Digital domain : Agilent Ptolemy**
 - signal processing simulations
- ❑ **Analogue domain : Circuit Envelope or High-Frequency SPICE (Transient) simulators**
 - analogue/RF simulations
- ❑ **Co-simulation : Agilent Ptolemy**
 - “master” for global co-simulations



MAIN ISSUES

- ❑ **HW/DSP/HW co-design**
 - RF implementation
 - Digital Signal processing algorithm
 - VHDL implementation
- ❑ **Validation of very closed functionality which strongly impact the global characteristics of the complete chain**
- ❑ **Architecture assessment regarding system requirements**



OVERVIEW OF THE ENVIRONMENT

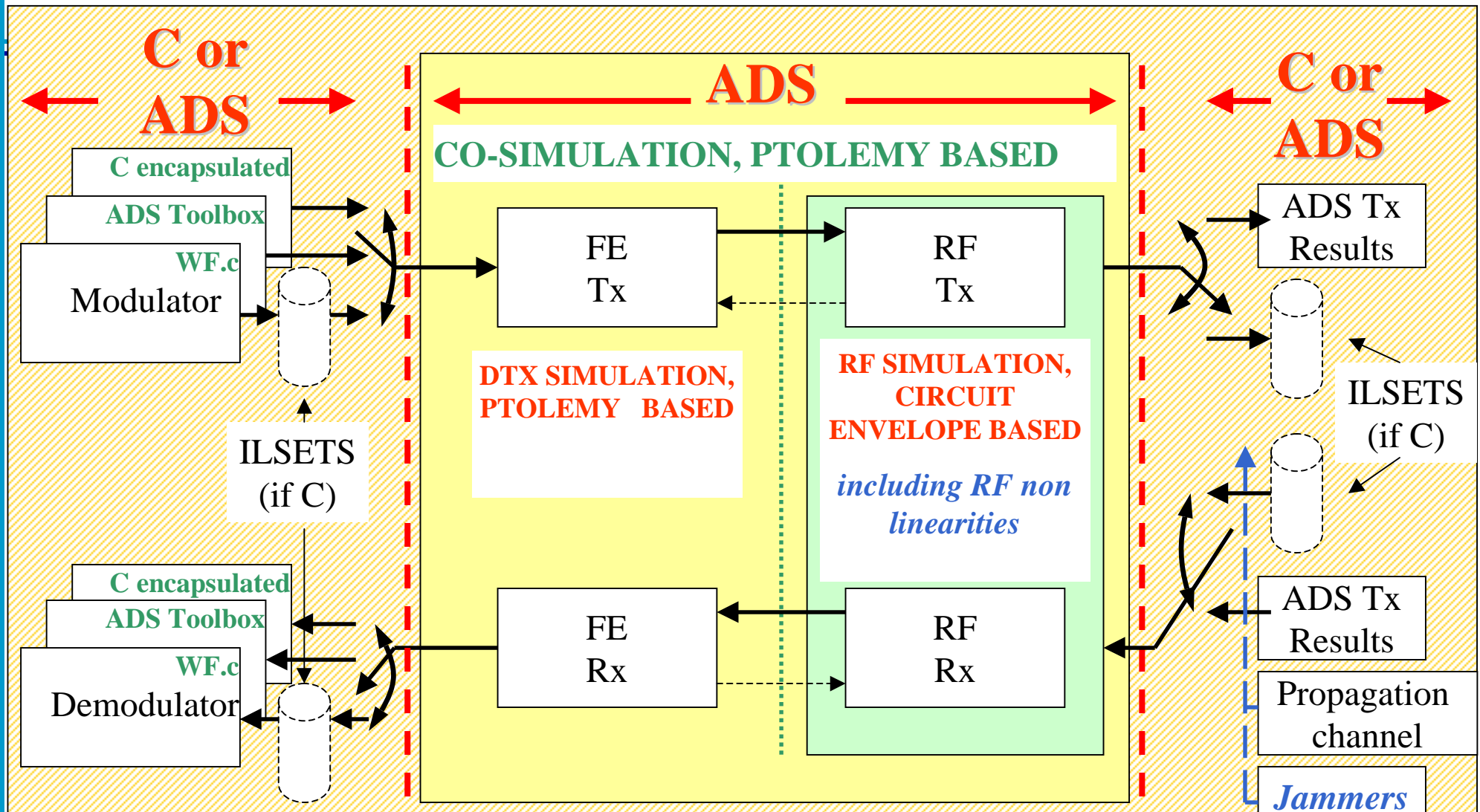


Figure A508
Spec - A508



FIRST SIMULATIONS

□ First step: independent simulations of both digital and RF chains

- Simulation of the analogue chain (with circuit envelope): RF and IF parts
 - simulates: amplifiers, mixers, oscillators, feedback loops... in the presence of modulated and transient high frequency signals
 - speed, efficiency and realistic details
 - includes: adjacent channels, harmonics, noise, ...
- Simulation of the digital chain (with Ptolemy): IF and BB parts
 - good performances
 - includes: ADC, digital filters, harmonics, ...



ADVANCED SIMULATIONS

□ Second step: co-simulation of digital and RF chains (plus propagation channel)

- The real added value is for feedback loops (Rx: AGC, Tx: Power control) between both worlds and simulations at different time scale levels with associated models:
 - RF: characterisation of non-linearities, ...
 - IF: AGC transient analysis
 - BB: long BER computations (see remark next slide), false alarm probability



3 - Advantages and drawbacks according to the needs



ADVANTAGES

- ❑ **Co-simulation between RF part and Digital Signal processing module**
- ❑ **Simulation of feedback loops**
 - Rx : AGC (ex digital filtering)
 - Tx : Power Control (ex linear PA for EDGE or UMTS)

- ❑ **Integration of the global environment**
 - non-linearities
 - jammer
 - Channel characteristics



DRAWBACKS/LIMITS OF ADS

❑ Extreme frequencies

- If we consider a co-simulation with the RF in the UHF band (225-400MHz) and if we want to simulate the effects of a closed interferer (for example at 25kHz of the useful signal), then the ratio between the extreme frequencies is 16000 (400MHz/25kHz) and ADS cannot perform the simulation in such conditions.

❑ Not suitable for BER simulation

- Too long $10^{-5} = \text{days}$, 1 ms = 4 days

❑ ADS Models

- Different ADS blocks + noise
- Not yet validated



4 - Current status



Current status

- ❑ **ADS is powerful but**
 - the simulation of the entire chain may be very long,
 - And expensive

- ❑ **Solution is applicable in small runs to validate particular concepts (eg: AGC, ALC...with transient issues)**

- ❑ **Classical approach seems more suitable for characterisation**
 - in C language or Matlab for instance

- ❑ **Both approaches are complementary**

- ❑ **Generation of VHDL test vectors to be assessed**



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