“Interfacing concept for different levels of abstraction in IP-based SoC design“

by

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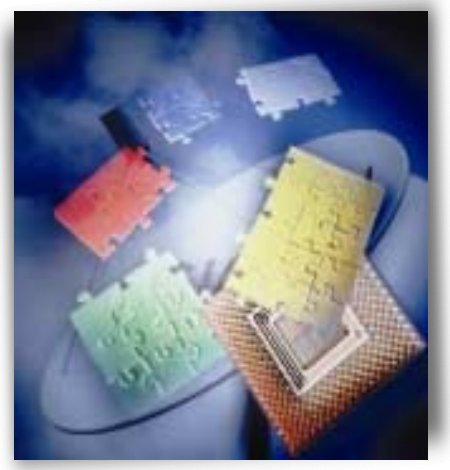

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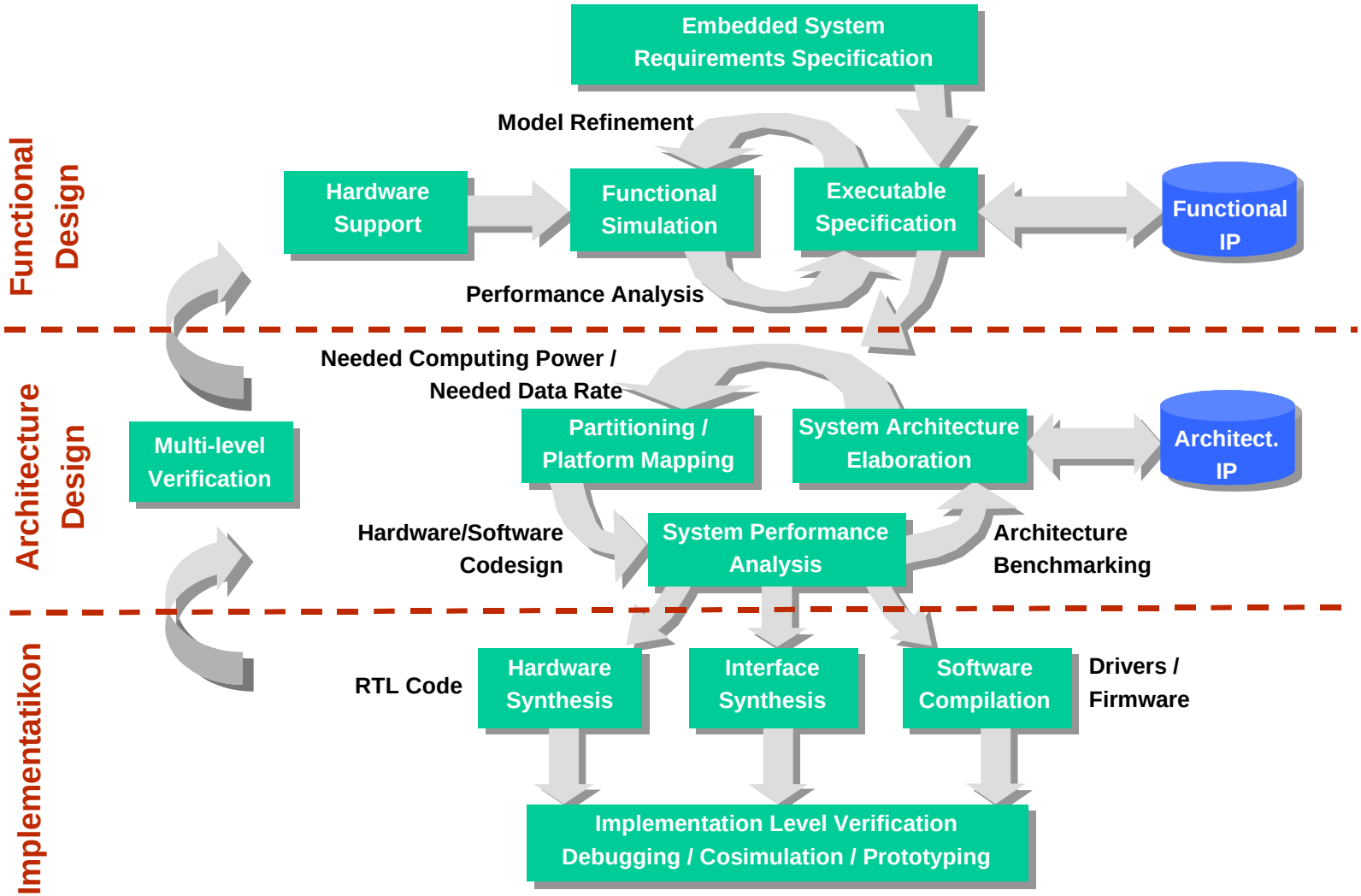
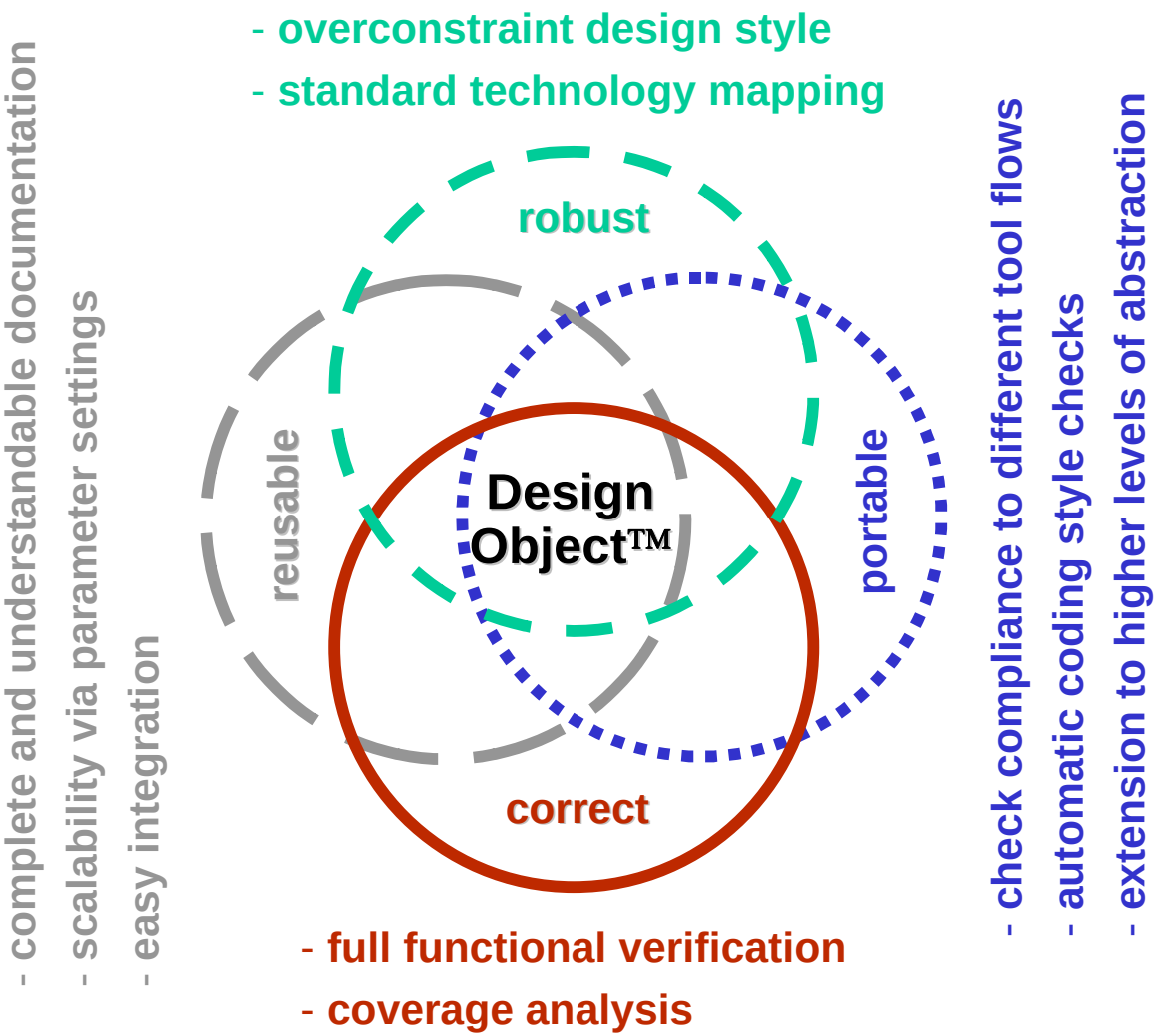
System-level Design Flow



IP Core Design Challenges



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Standardization Activities in System-level Design

gain compatibility by standarization of:

- (open) modeling languages and extensions
  - systemC, Superlog, Java, UML-RT, SDL, e-Language, OpenVera, Testbuilder,..
- documentation structure
  - explaining documents format templates, ease understanding and utilization
- deliverables data formats
  - source code, models, specifications, reports, scripts,..
- architecture and interfacing
  - test structures, on-chip bus standards,..

Virtual Socket Interface Alliance

www.vsi.org

- founded in September 1996
- purpose: “encouragement of virtual component transfer and SoC integration”
- currently about 175 member companies
- different development working groups
  - system-level design, on-chip bus, VC quality, AMS, IP protection, VC transfer, impl. Verification, functional verification, manufac. test
- established different specifications, among those:
  - Deliverables document (DD 2.x)
  - System-Level Interface Behavioral Documentation Standard Version 1 (SLD 1 1.x)
  - Virtual Component Interface Standard Version 2 (OCB 2 2.x)

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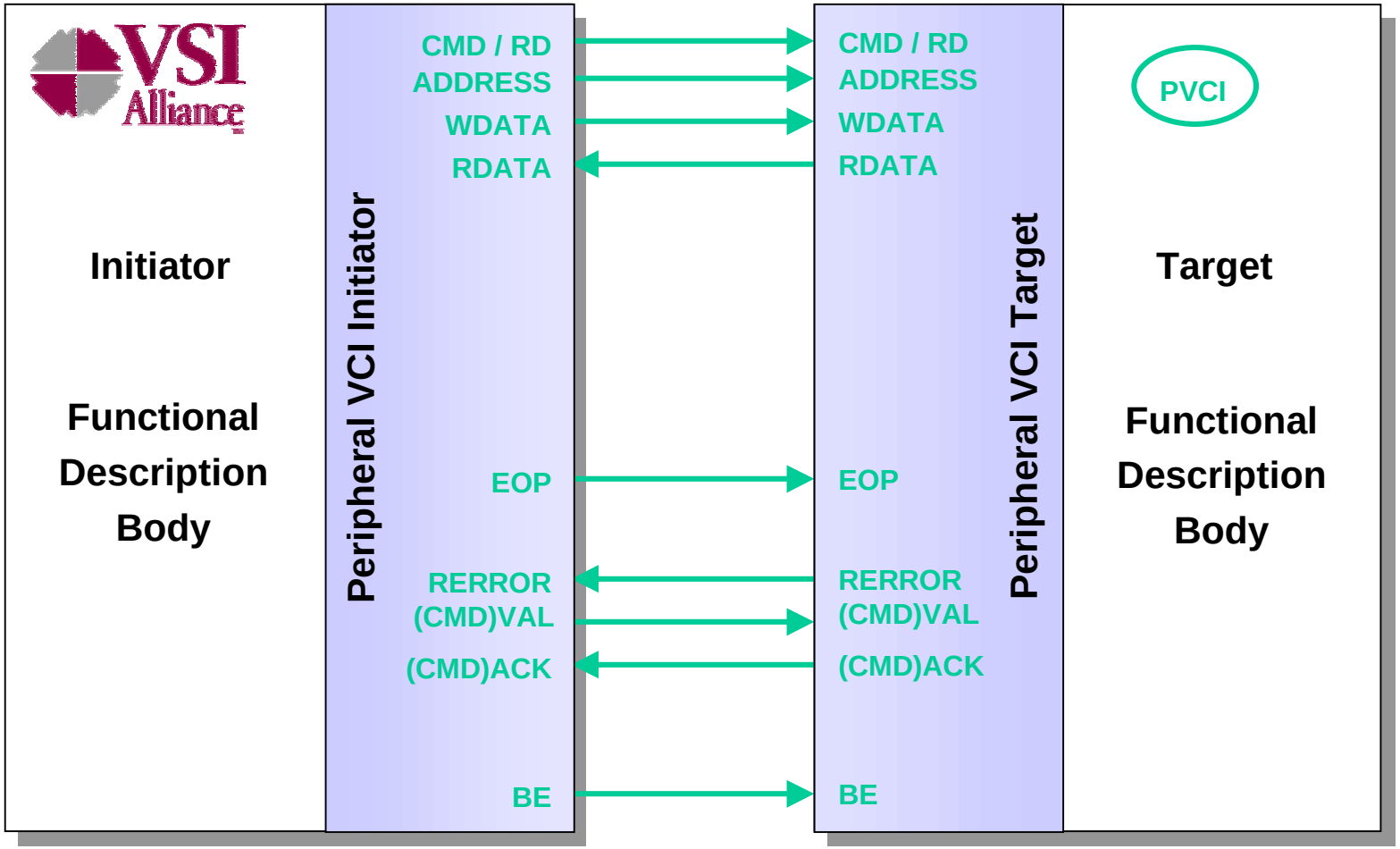
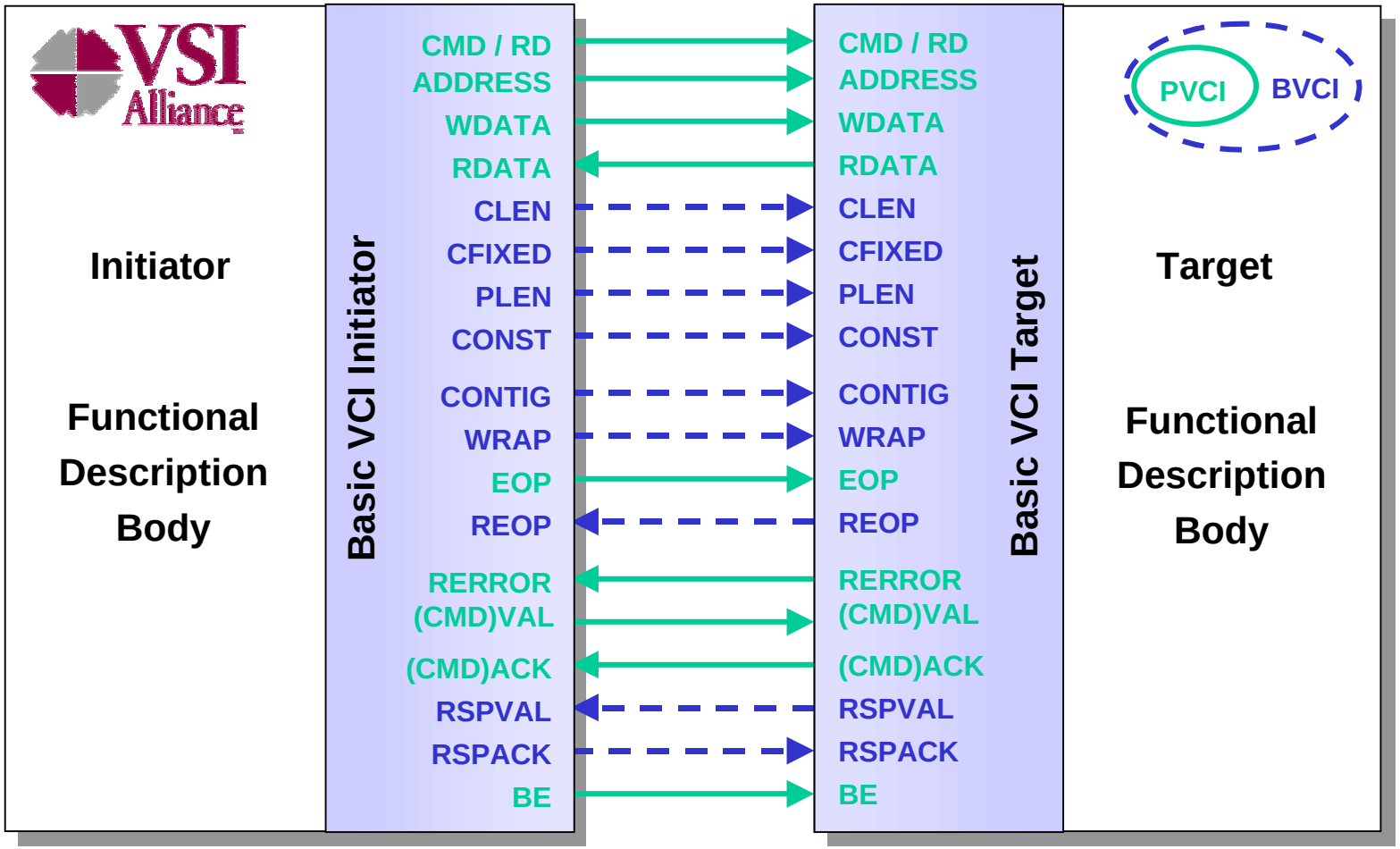
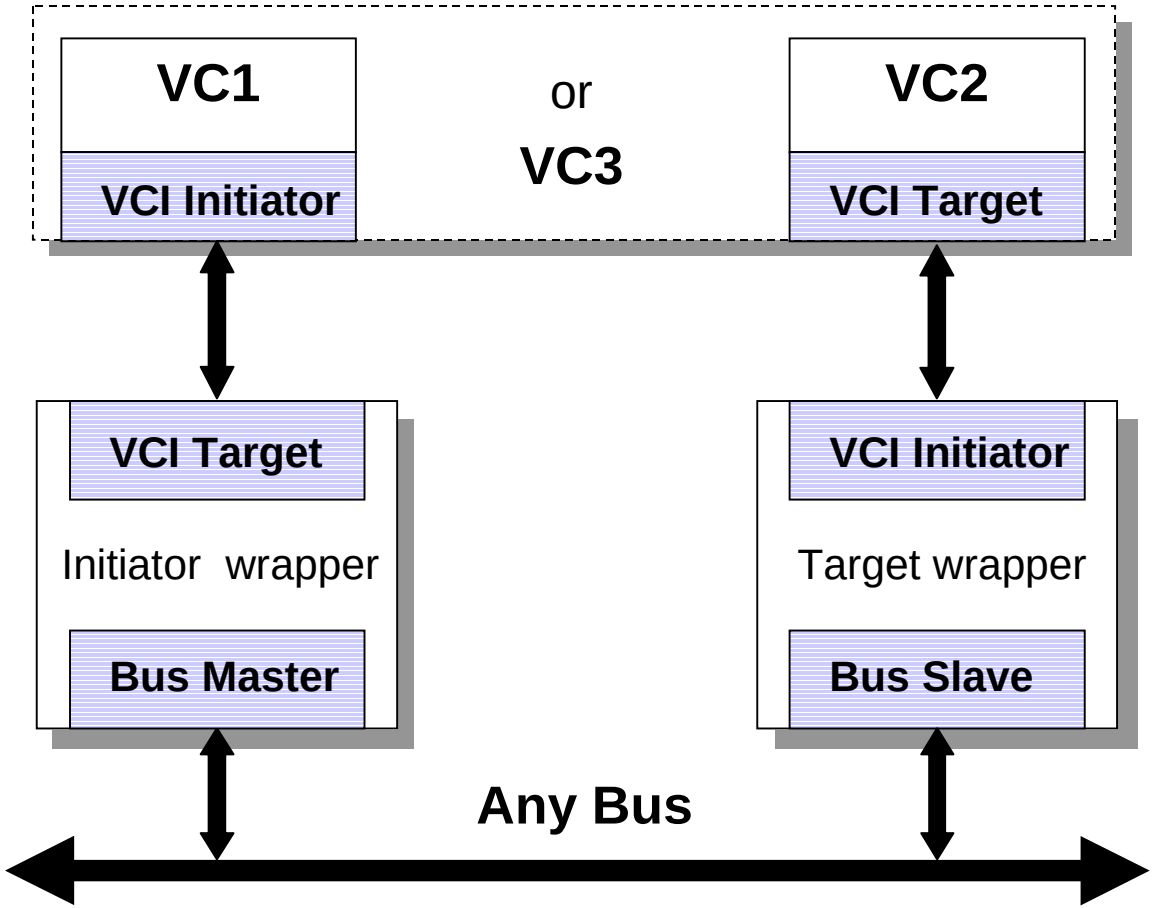
Peripheral Virtual Component Interface



Basic Virtual Component Interface



VCI Uni-level Interface Adaptation



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Investigation Goals and Limits

multi-abstraction level system-IP design

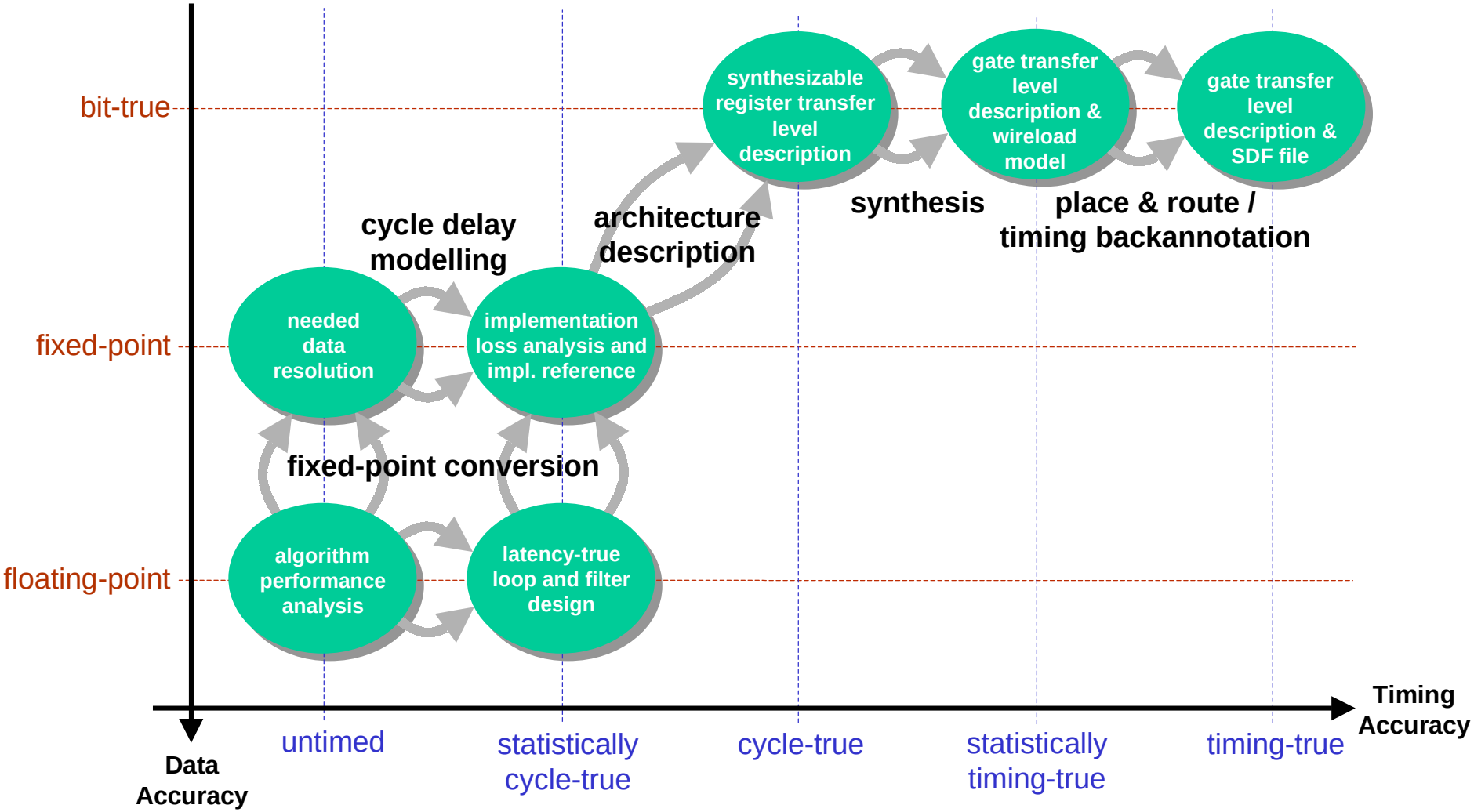
- first goals/interests
  - smooth model transition during functional and architectural design
  - gain VSIA compliance as far as possible
- framework
  - ***Spe****cification and* ***A****lgorithm/****A****rchitecture* ***C****o-Design...*
  - task 3.3 system-IP design
- limits
  - levels over and including RTL
  - initial focus HW module development at different levels of abstraction
- open issues
  - software appliance check
  - synchronization: software function – RTOS – HDL description
  - definition of mandatory used subset of model classes/combinations

System-level Model Classification I

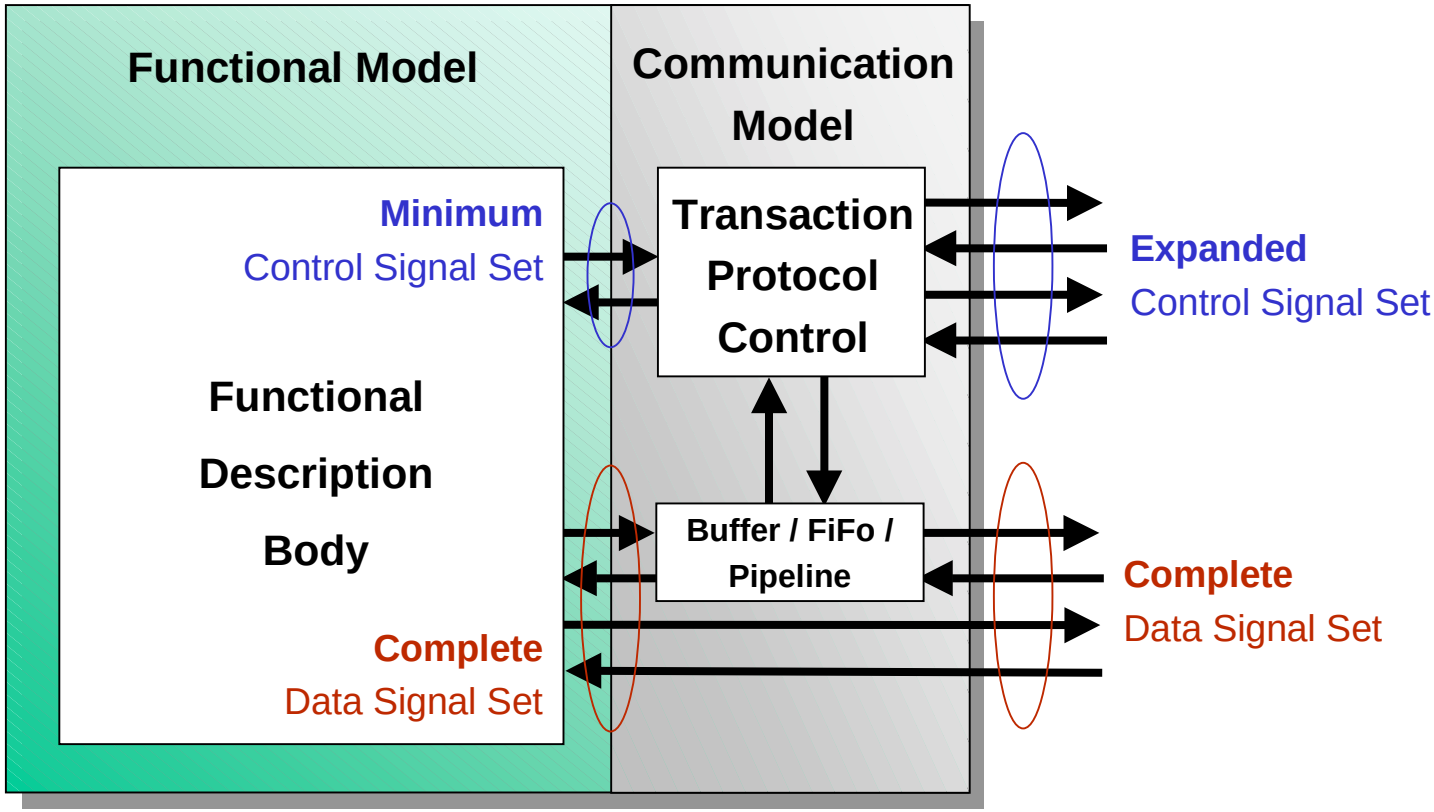
categories:

- data accuracy
  - floating-point / fixed-point, integer / bit-true
- timing accuracy
  - untimed / statistical delay / clock cycle true
- communication accuracy
  - transaction-based / packet-based / cell-based
  - data flow / control flow
  - dedicated point-to-point / bus connection point-to-multipoint
  - blocking / non-blocking
  - data priority / control priority
  - non-buffered / buffer / fifo / pipeline

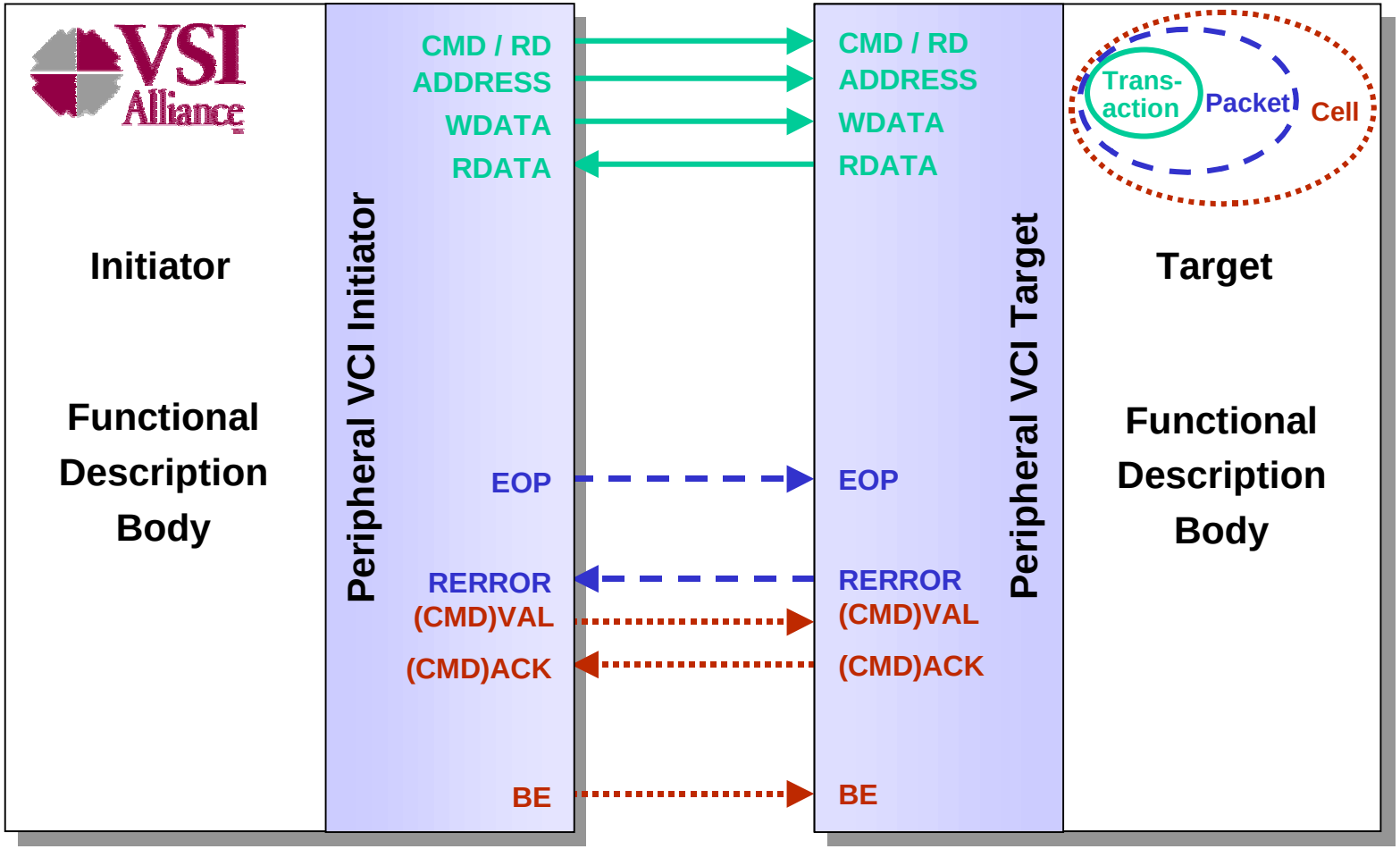
System-level Model Classification II



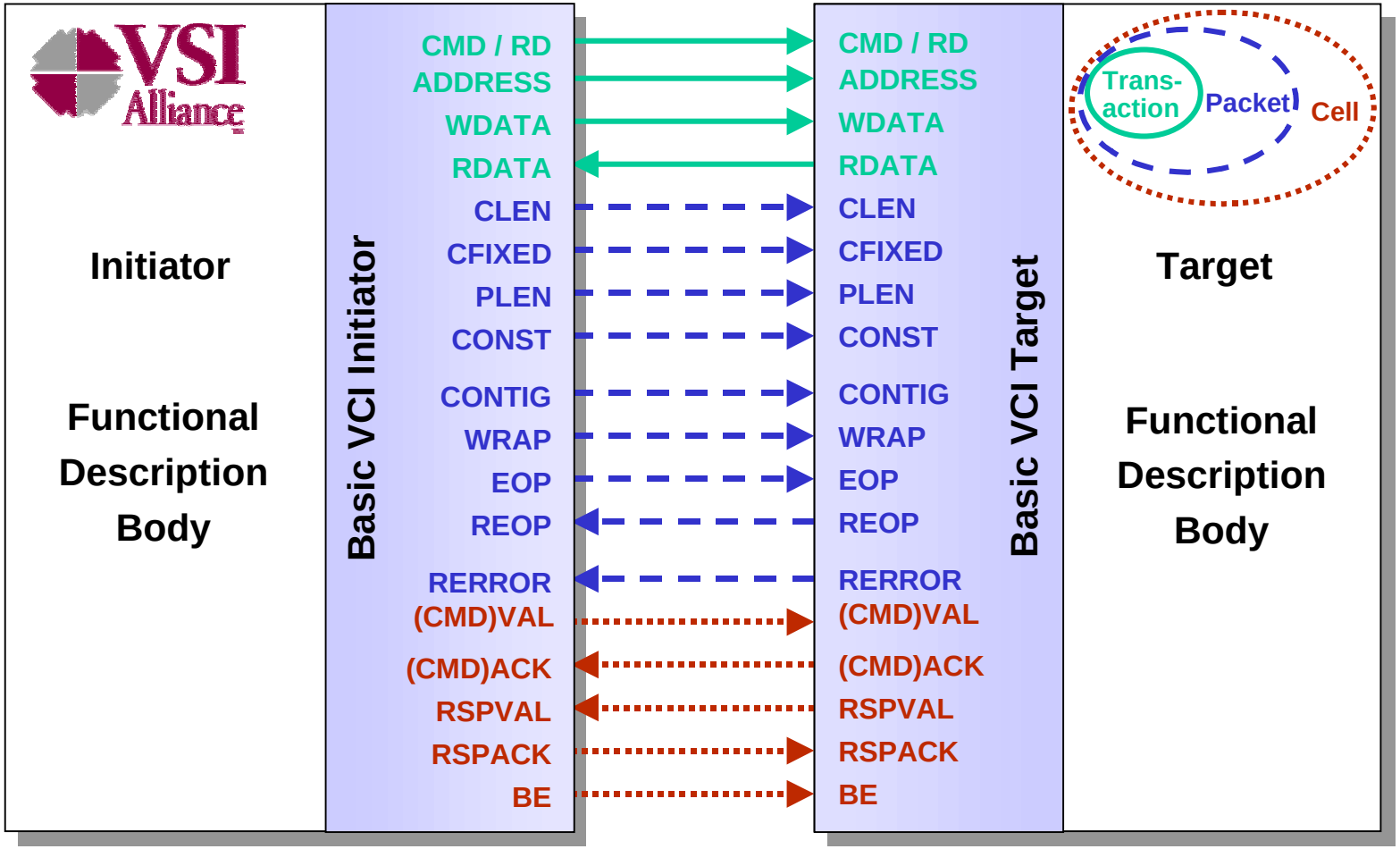
System-level Model Classification III



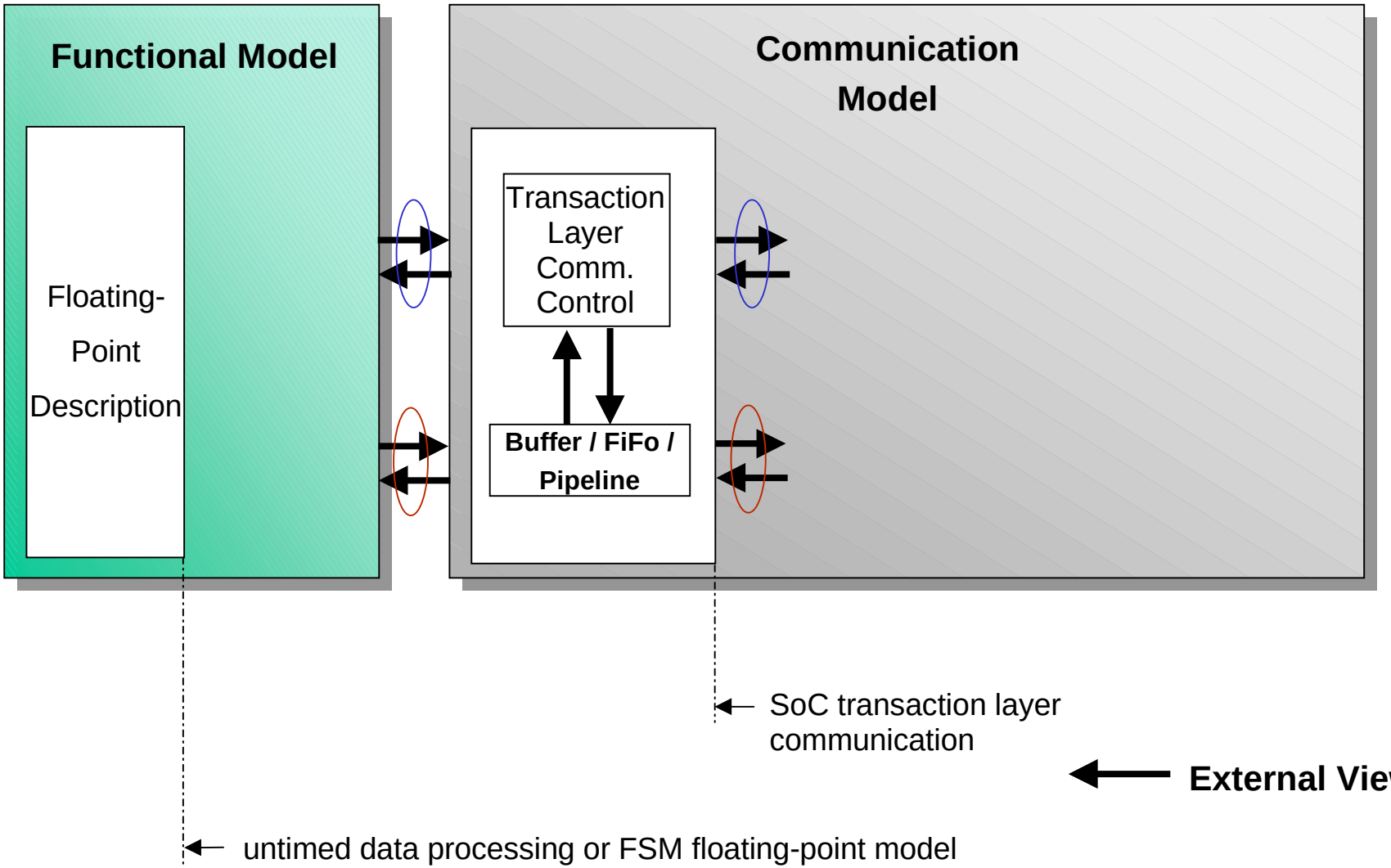
Peripheral VCI at Different Communicat. Levels



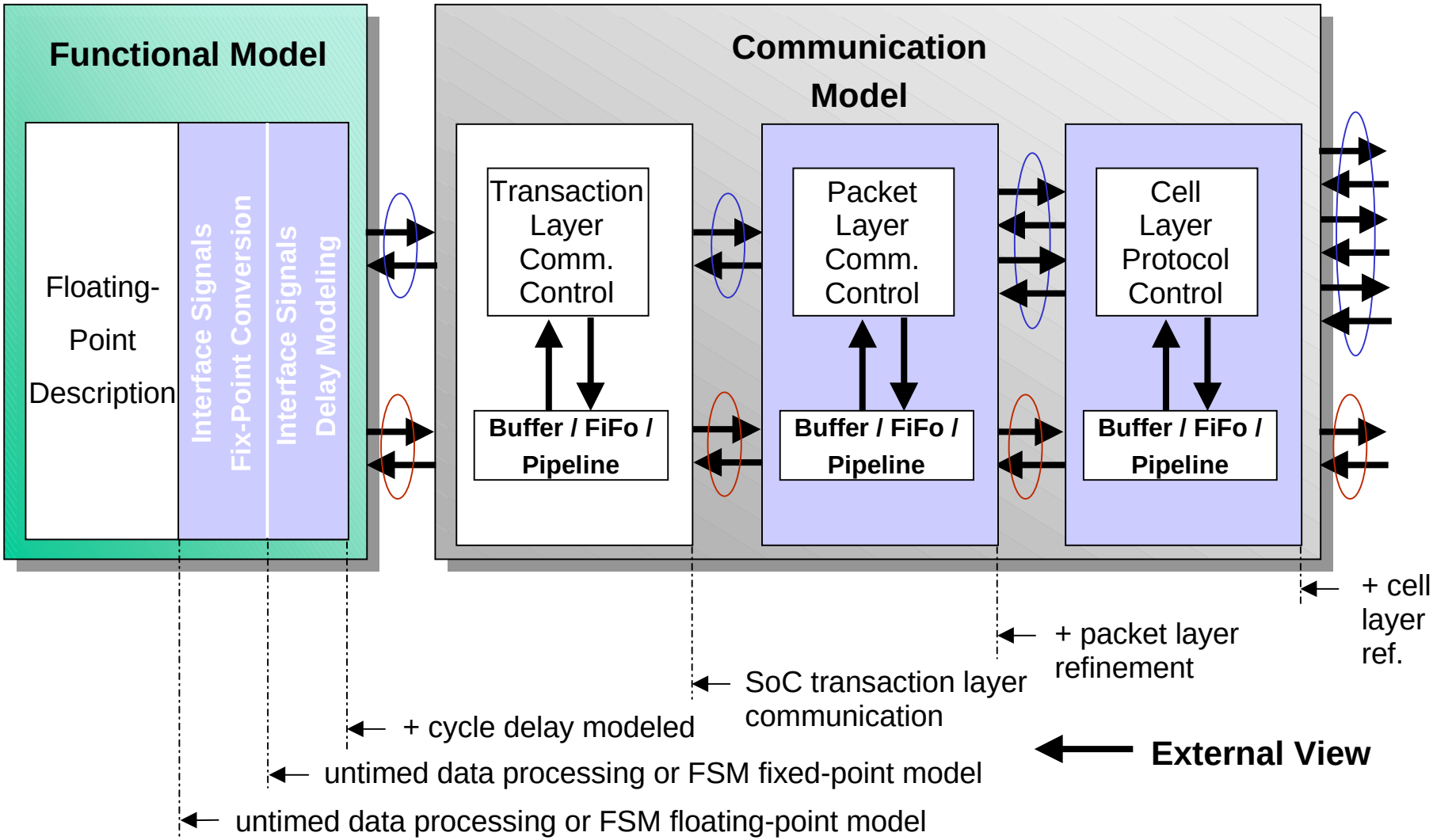
Basic VCI at Different Communication Levels



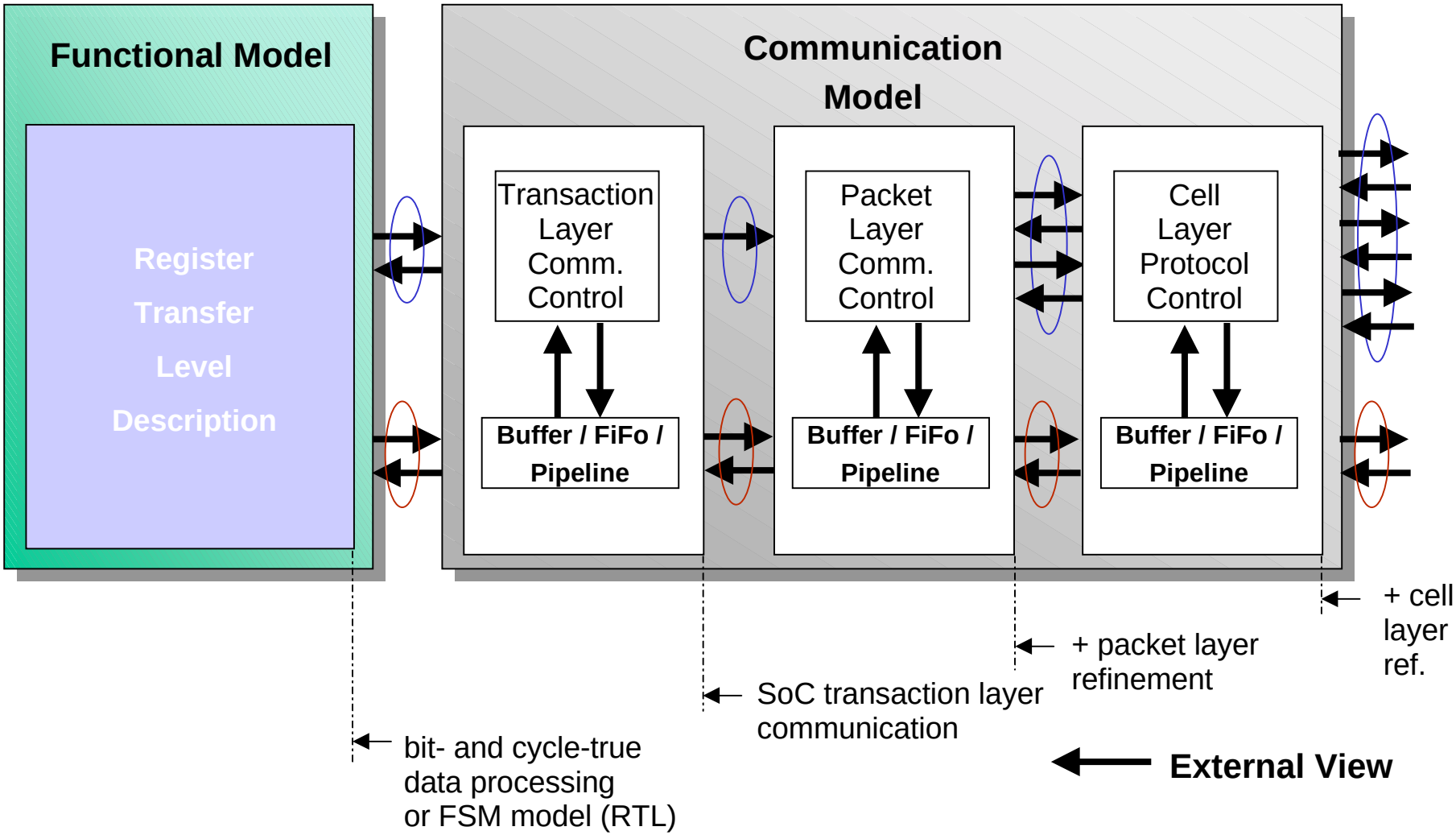
Multi-level Interface Wrapping Example I



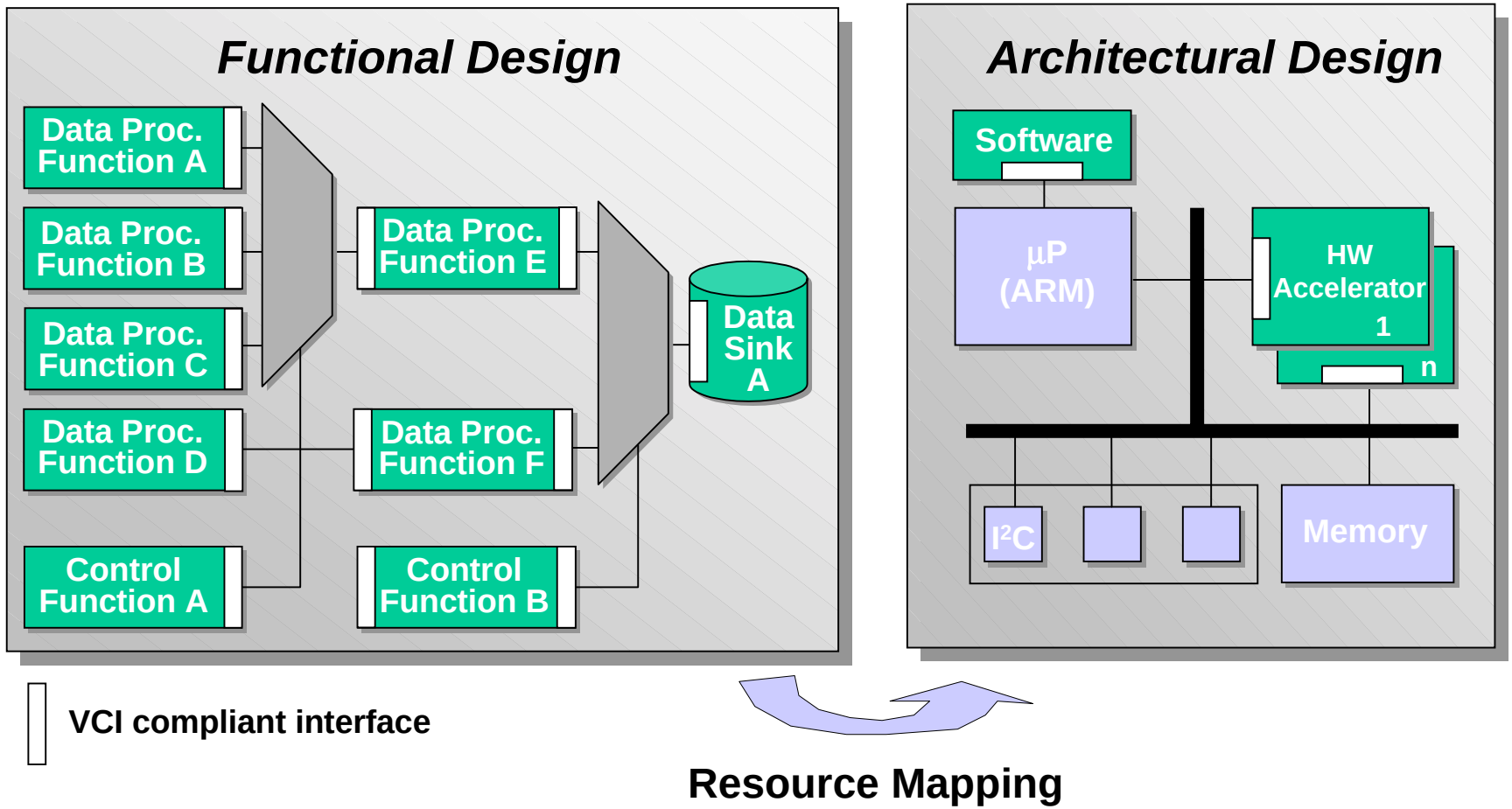
Multi-level Interface Wrapping Example II



Multi-level Interface Wrapping Example III



System-on-Chip Example

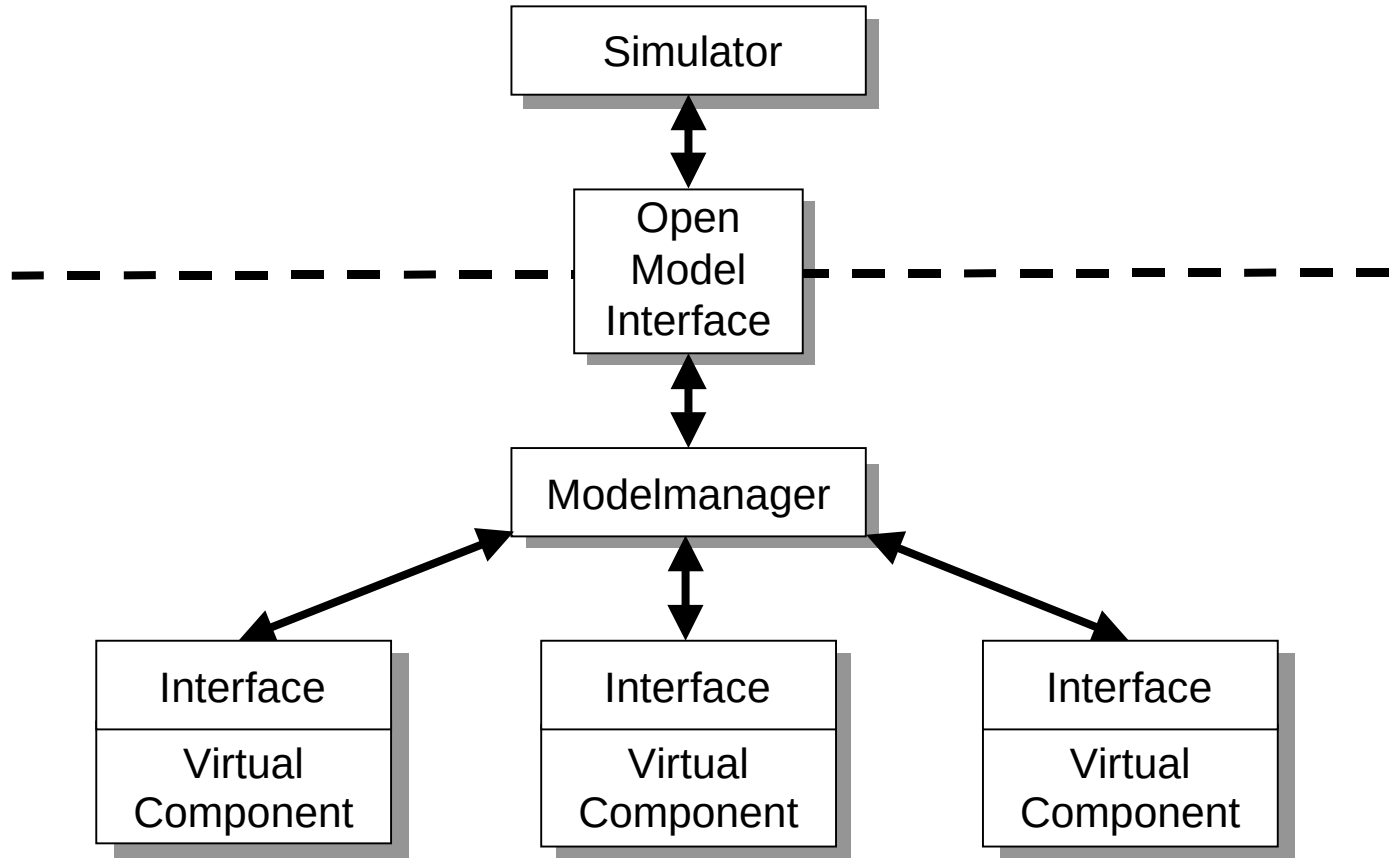


Portability Securing I

open model interface (IEEE Std 1499-1998) features

- standard IF for model-to-simulator link
- mixed-language model simulation capability
  - VHDL, Verilog, ANSI-C
  - advantage over PLI, Verilog-only standardized
- different model boundary classes and data types
  - port, parameter, viewport
  - 2-/4-state logic, booldean, integer, string, real
- simulator minimum capability definition
  - two-state boundary data class, cycle-based simulation style
- simulator stages of execution
  - bootstrap, elaboration, initialization, simulation, termination

Portability Securing II



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Outlook

next steps and open issues

- implementation of the concept in SystemC
- check appliance for tools (SystemStudio, VCC,..)
- definition of mandatory used subset of model classes/combinations
- software appliance check
- synchronization: software function – RTOS – HDL description

Conclusion

- Motivation and Goals
  - systen level design flow, IP design challenges
- Development Framework
  - standardization activities, VSI Alliance
- Interfacing on Register Transfer Level (RTL)
  - peripheral VCI, basic VCI, uni-level interface adaptation
- Interfacing on Levels over RTL
  - investigation goals and limits
  - system-level model classification
  - peripheral and basic VCI at different communication levels
  - multi-level interface wrapping example
  - system-on-chip example
  - portability securing, open model interface

References

- [1] *Virtual component interface standard*, version 2.0 (OCB 2 2.0), by the On-chip Bus Development Working Group of the VSIA (www.vsi.org), April 2001
- [2] *System-level interface behavioral documentation standard*, version 1.0 (SLD 1 1.0), by the System-level Design Development Working Group of the VSIA (www.vsi.org), March 2000
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- [7] *SpeAc project homepage*, http://speac.fzi.de