Studies on Instruction Set Emulation for the Rapid Prototyping of SoCs

Jürgen Schnerr (FZI, Universität Tübingen)
Wolfgang Rosenstiel (FZI, Universität Tübingen)
Rainer Kress (Infineon)

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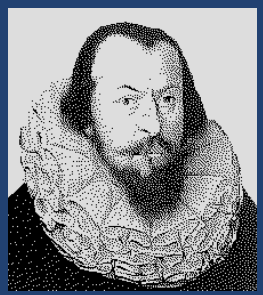

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J. Schnerr
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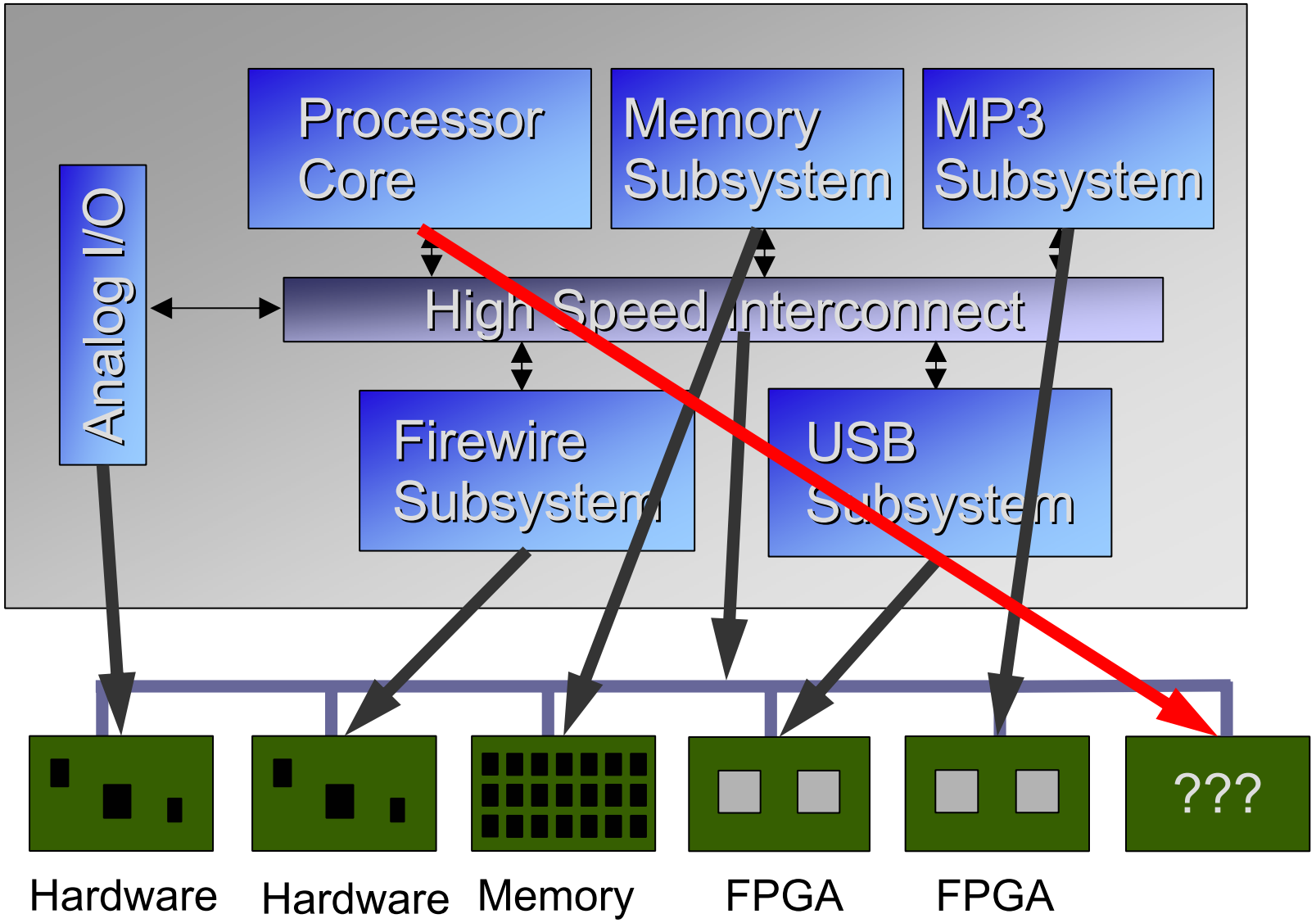

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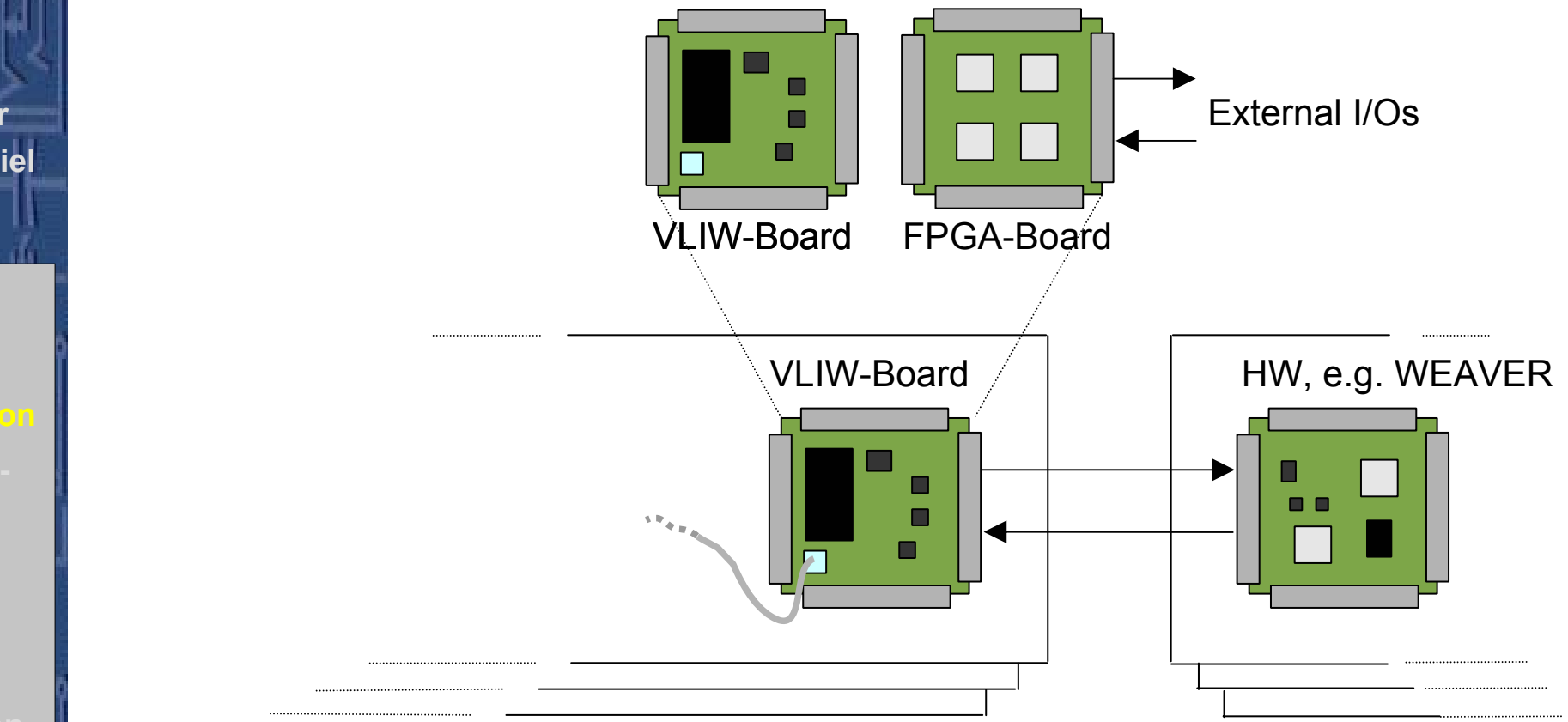
Emulation of SoCs/2



ISS: Instruction Set Simulation
BFM: Bus Functional Model

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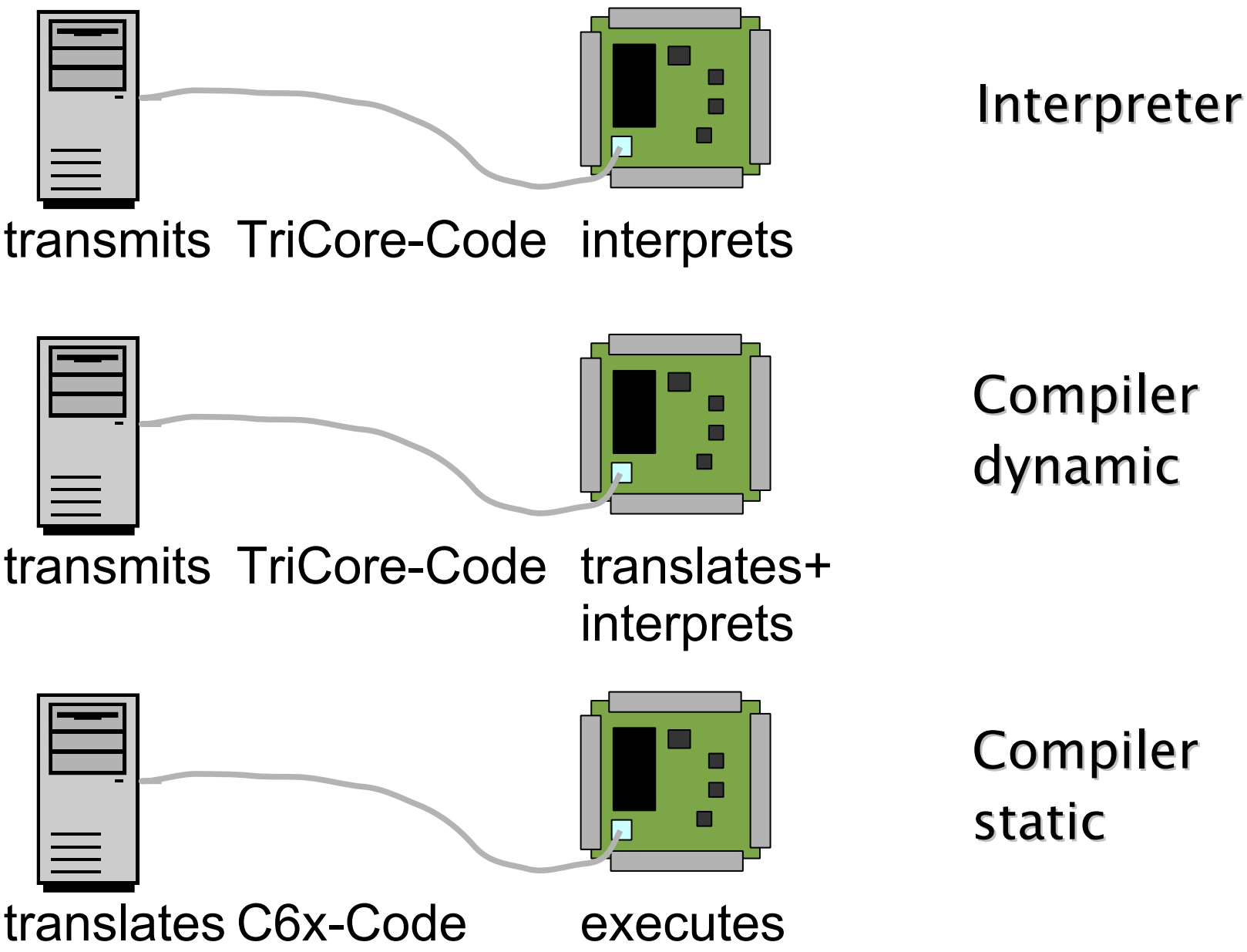
Reproduction of SoC-Object Code



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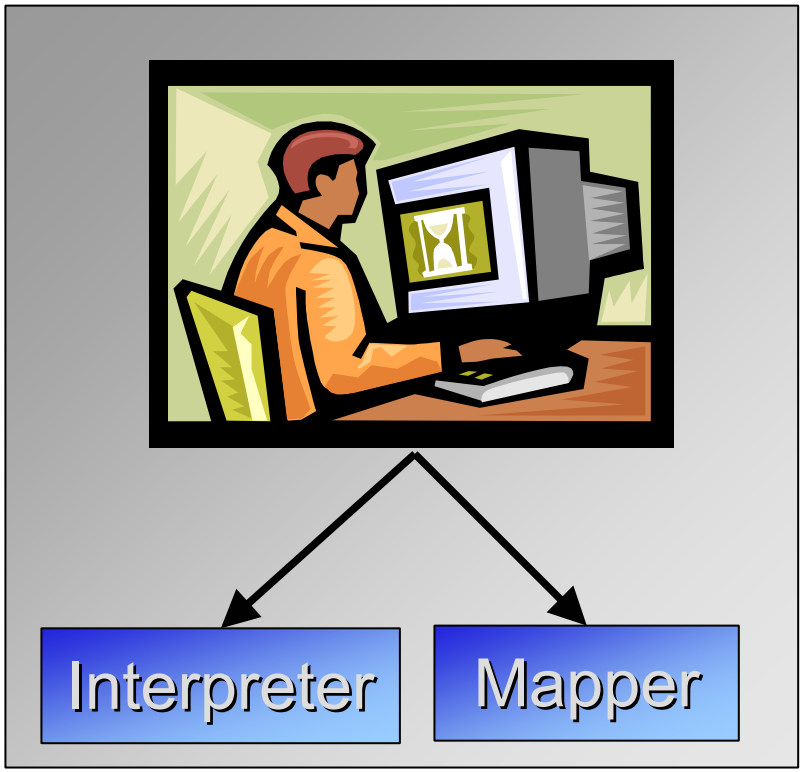
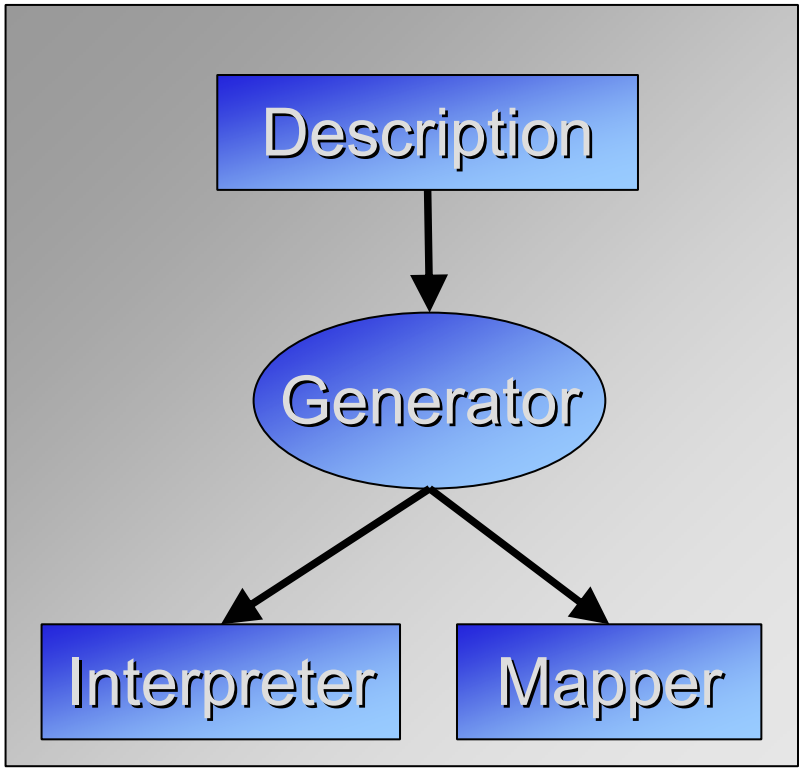
Generation of the Interpreter/Mapper

2 fundamental possibilities





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Structure of an Interpreter

Fetch the instruction

```
instruction=(mem & 0xff000000) >> 24;
switch (instruction)
{
  /* 0x19 ld.w Da, [An]offset (BOL) */
  case 0x19:
```

Decode the parameters

Execute the Instruction

```
    break;
...
}
```

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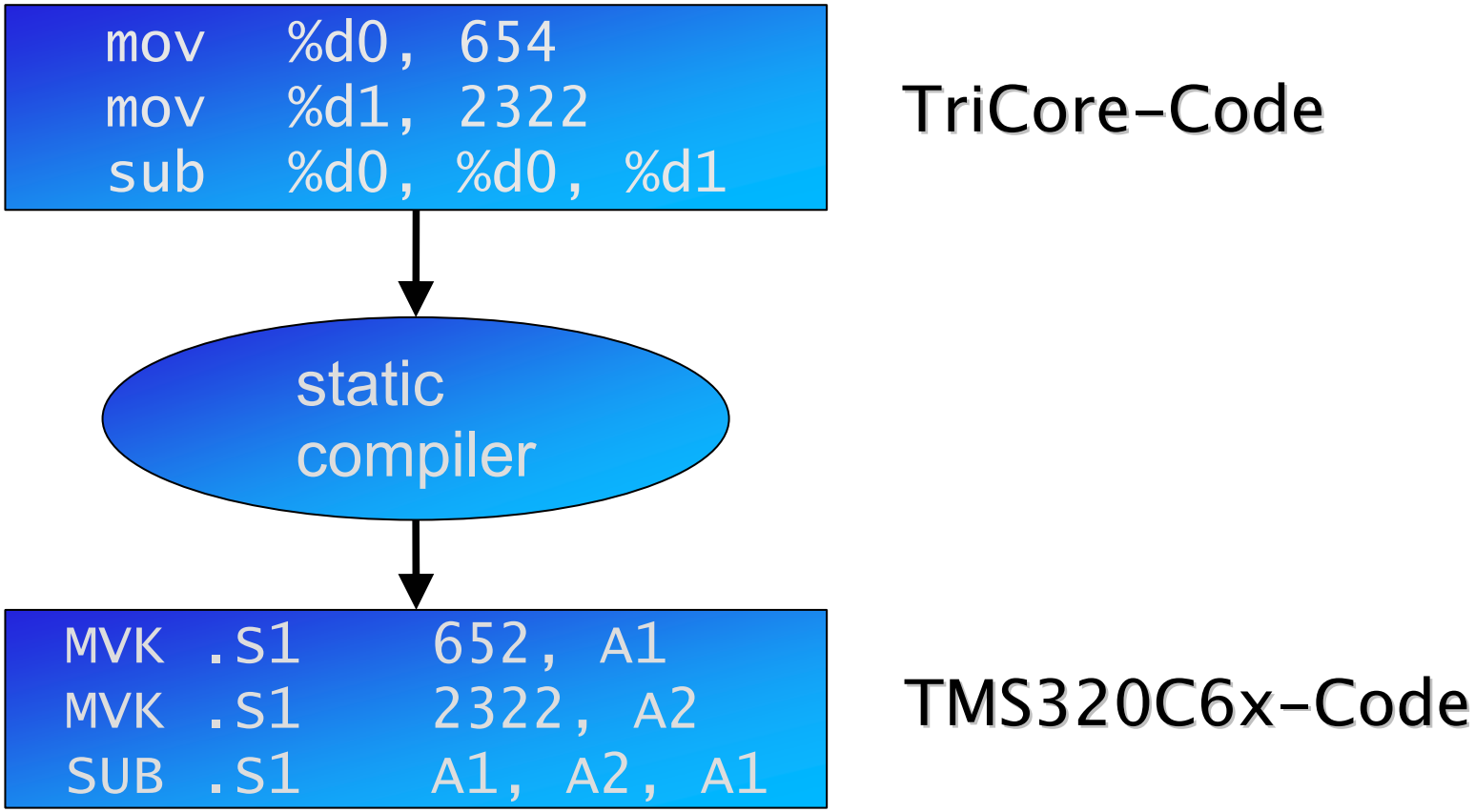
Functionality of the Mapper



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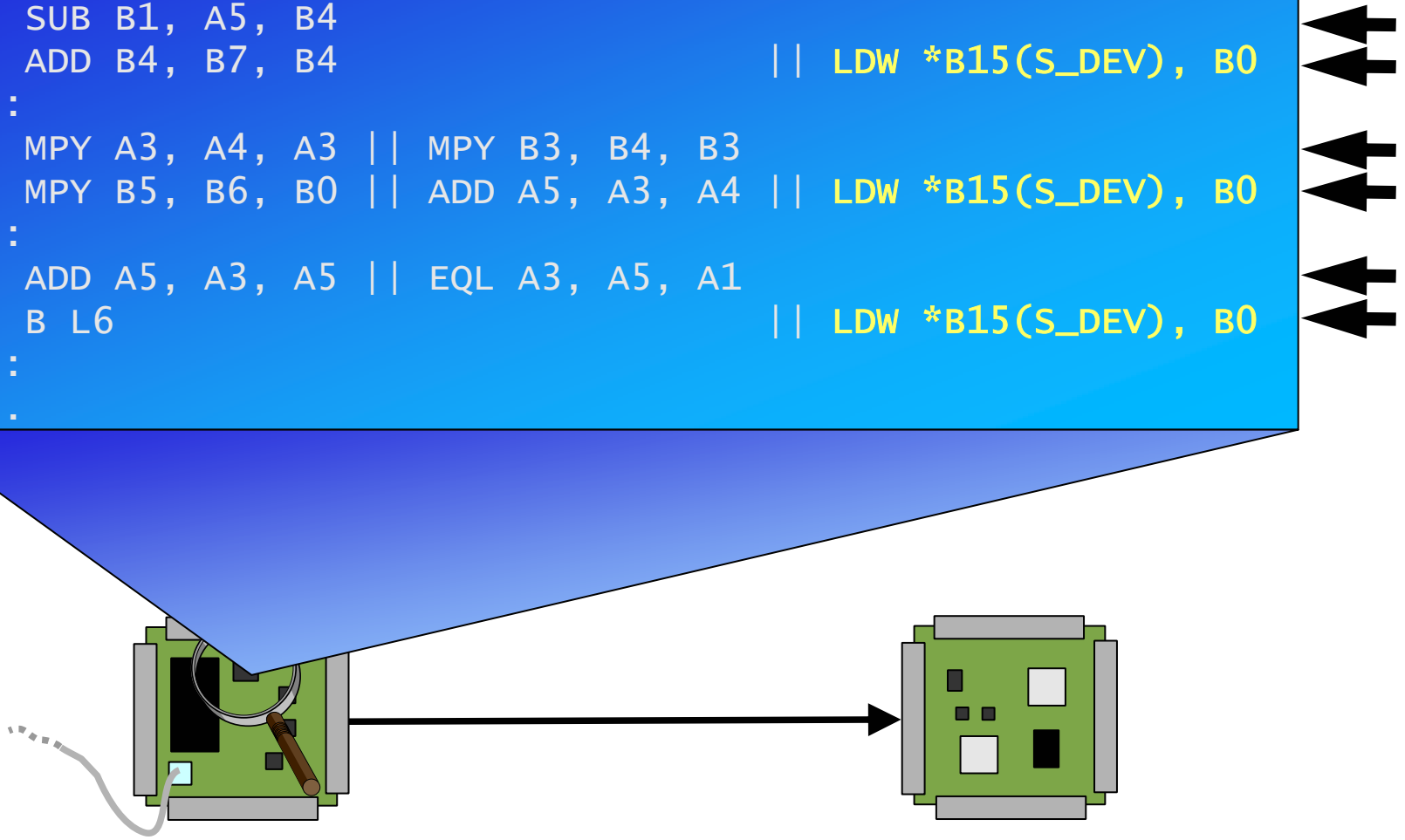
Synchronisation

```
...
L2:
   SUB B1, A5, B4
   ADD B4, B7, B4                          || LDW *B15(S_DEV), B0
L3:
   MPY A3, A4, A3 || MPY B3, B4, B3
   MPY B5, B6, B0 || ADD A5, A3, A4 || LDW *B15(S_DEV), B0
L4:
   ADD A5, A3, A5 || EQL A3, A5, A1
   B L6                                    || LDW *B15(S_DEV), B0
L5:
...
```



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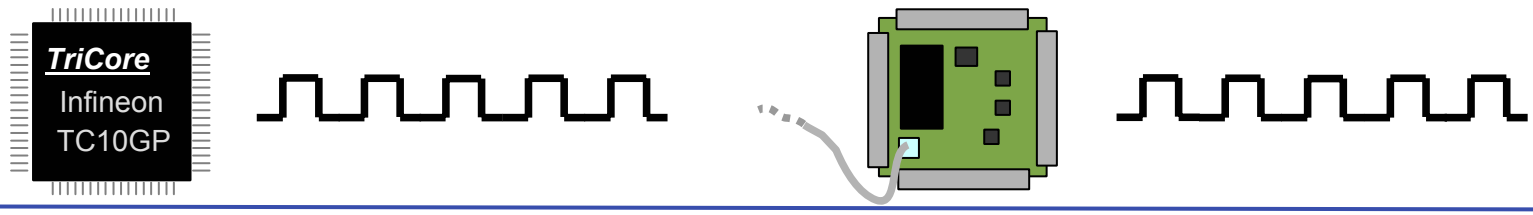
Cycle Accuracy

TriCore	TMS320C6x
`mov %d0, 654`	`MVK .S1 652, A1` `LDW *B15(S_DEV), B0`
`mov %d1, 2322`	`MVK .S2 2322, B2` `LDW *B15(S_DEV), B0`
`sub %d0, %d0, %d1`	`SUB .L1 A1, B2, A1` `LDW *B15(S_DEV), B0`

`swap.w %d0, .L2`	`MVK .S1 .L2, A10`
	`MVKH .S1 .L2, A10`
	`LDW .D1 *A10, A15`
	`STW .D1 A1, *A10`
	`MV .S1 A15, A1`
	`LDW *B15(S_DEV), B0`
	`LDW *B15(S_DEV), B0`



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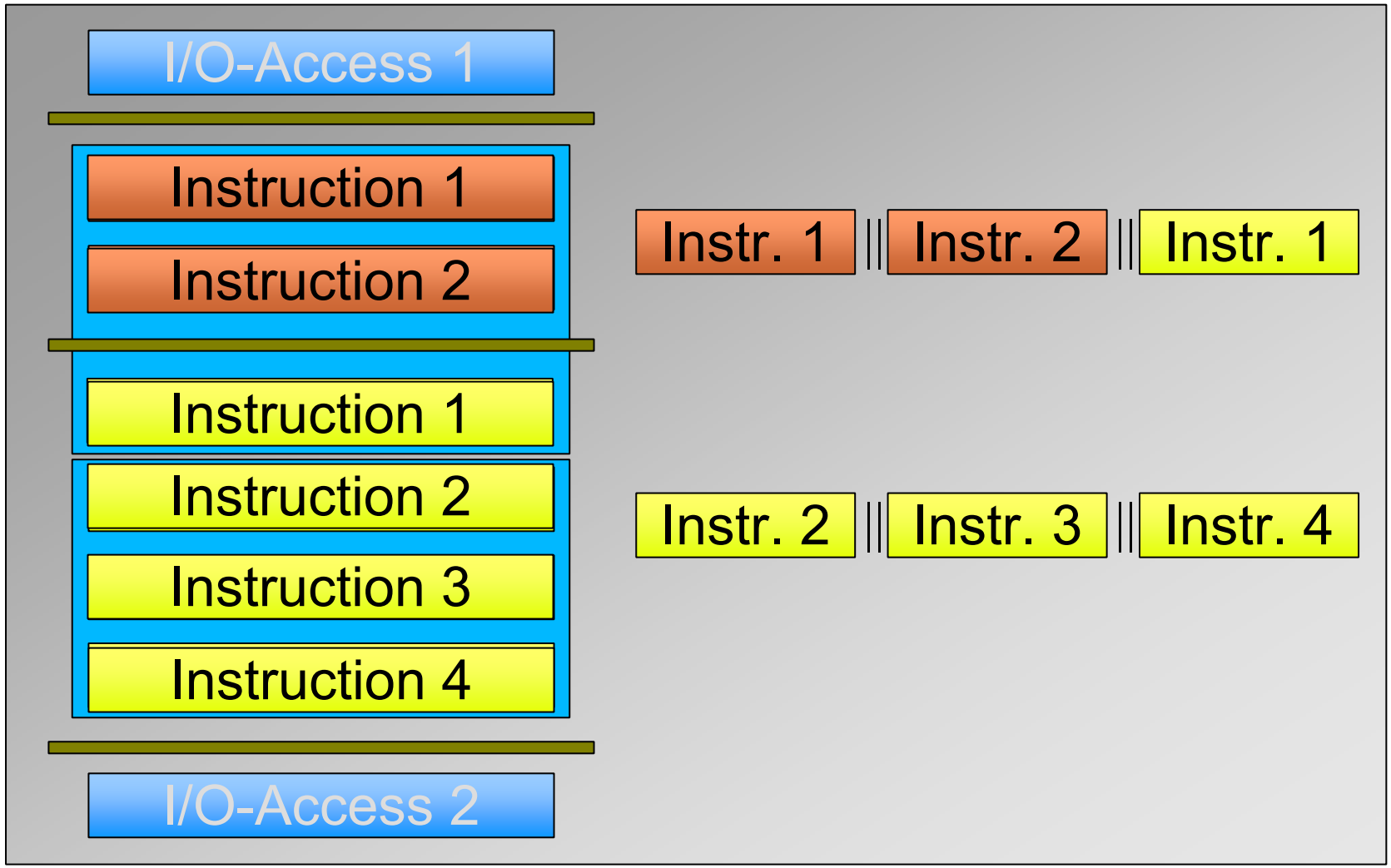
Optimisation



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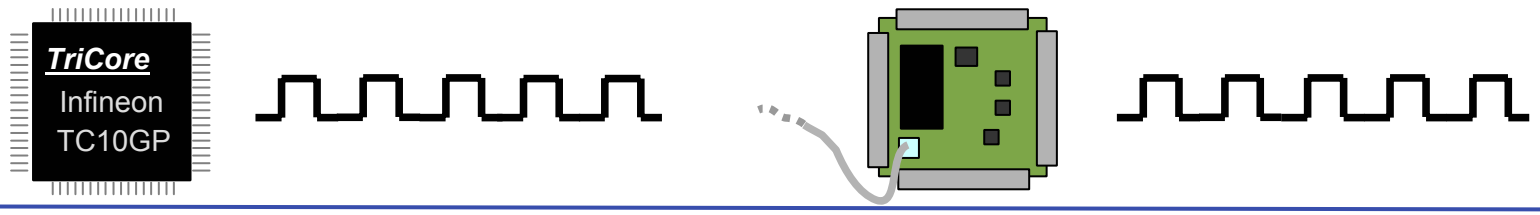
Multiple Synchronisation Cycles

TriCore	TMS320C6x
mov %d0, 654	STW A1,*B15(S_DEV+5) MVK .S1 652, A1 || MVK .S2 2322, B2
mov %d1, 2322	SUB .L1 A1, B2, A1 || MVK .S1 .L2, A10
sub %d0, %d0, %d1	MVKH .S1 .L2, A10 LDW .D1 *A10, A15
swap.w %d0, .L2	STW .D1 A1, *A10 || MV .S1 A15, A1 || LDW *B15(S_DEV), B0



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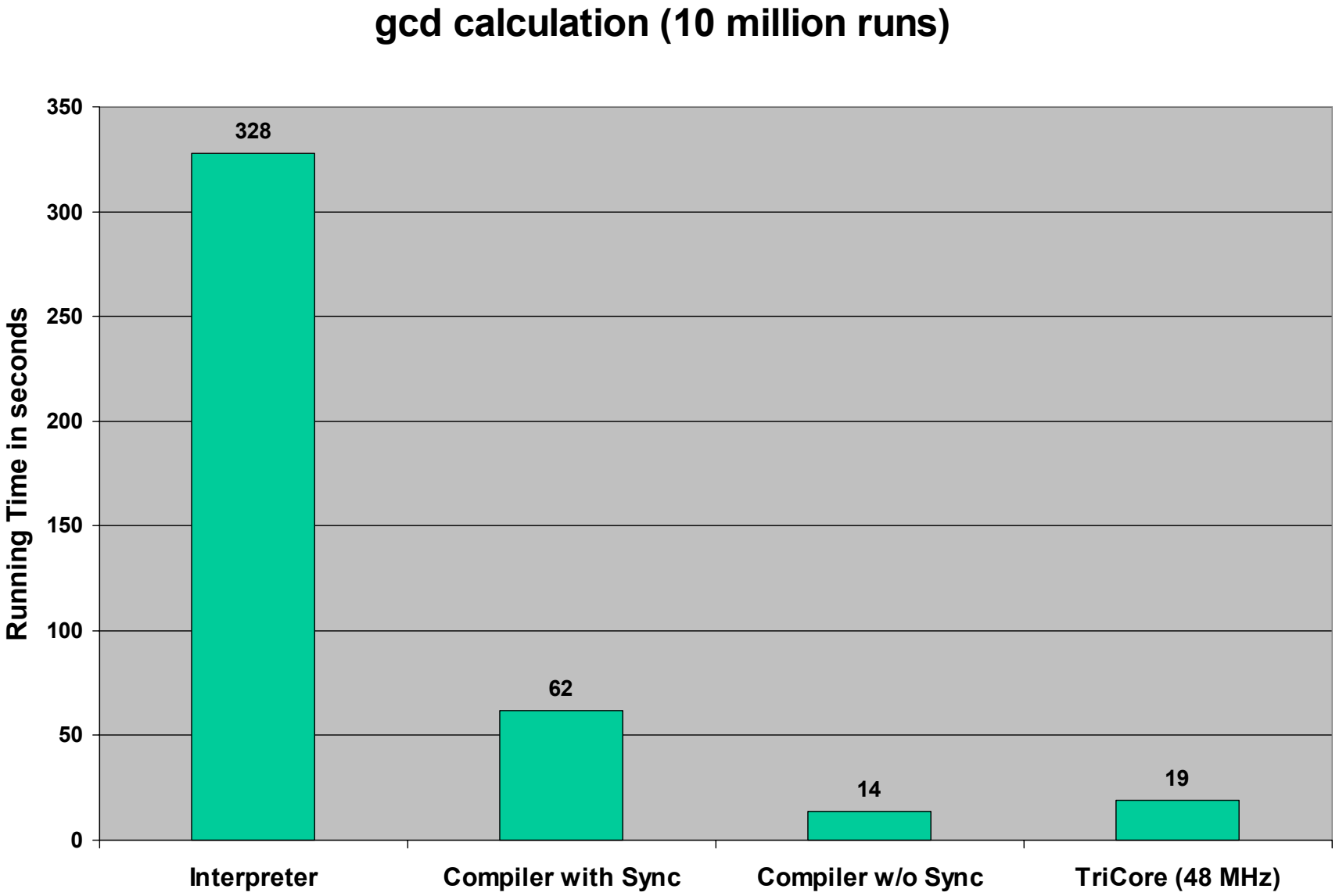
Results running gcd calculation



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Conclusion

- Existing problems in system prototyping of SoCs have been discussed
  ⇒ especially the problem of emulating the processor core
- The solution of this problem has been demonstrated
  ⇒ cycle accurate ISE on a board using a VLIW-processor
- Fundamental concepts for the implementation of this ISE have been presented
- First promising results with the system have been achieved