



Specification of multi-domain systems based on Matlab / Simulink

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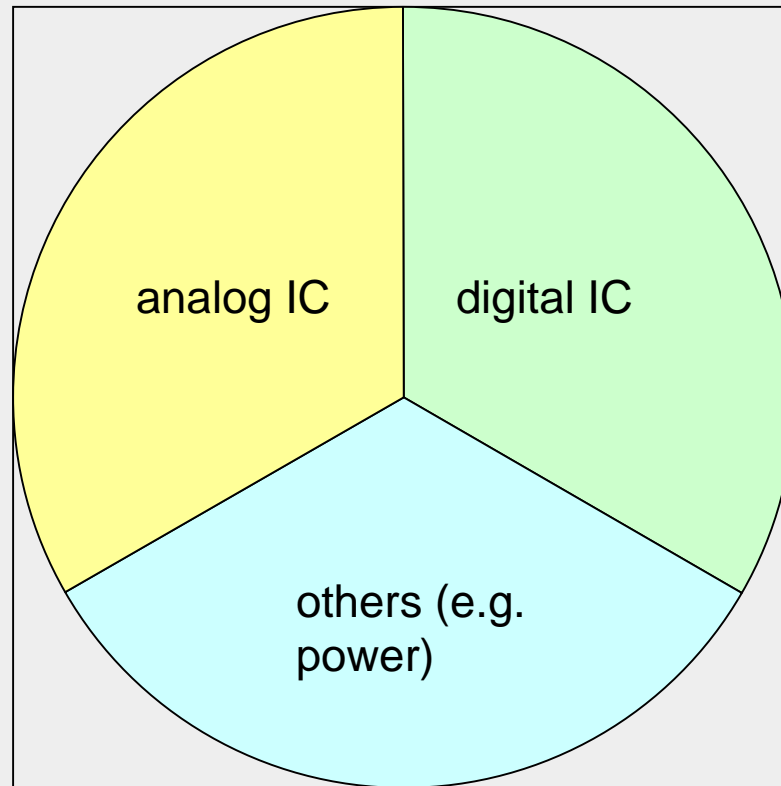
- Special requirements at Bosch
- Our project goals
- Activities and results
- Introduction of a system example
- Summary and outlook



- Automotive sector:
 - most designs with extremely high demands on security and reliability
 - special environment
 - ◆ extreme temperatures
 - ◆ mechanical shock
 - ◆ electromagnetical fields
 - integration for reduction of
 - ◆ size
 - ◆ weight
 - ◆ costs



- ASICs to meet special requirements
- Mostly BCD processes
- Designs from various domains with a wide range of complexity
 - Sensor control (micromechanical, analog, digital)
 - Airbag control (analog, digital)
 - Video sensing (digital, SW)
 - DAB (digital, high complexity)

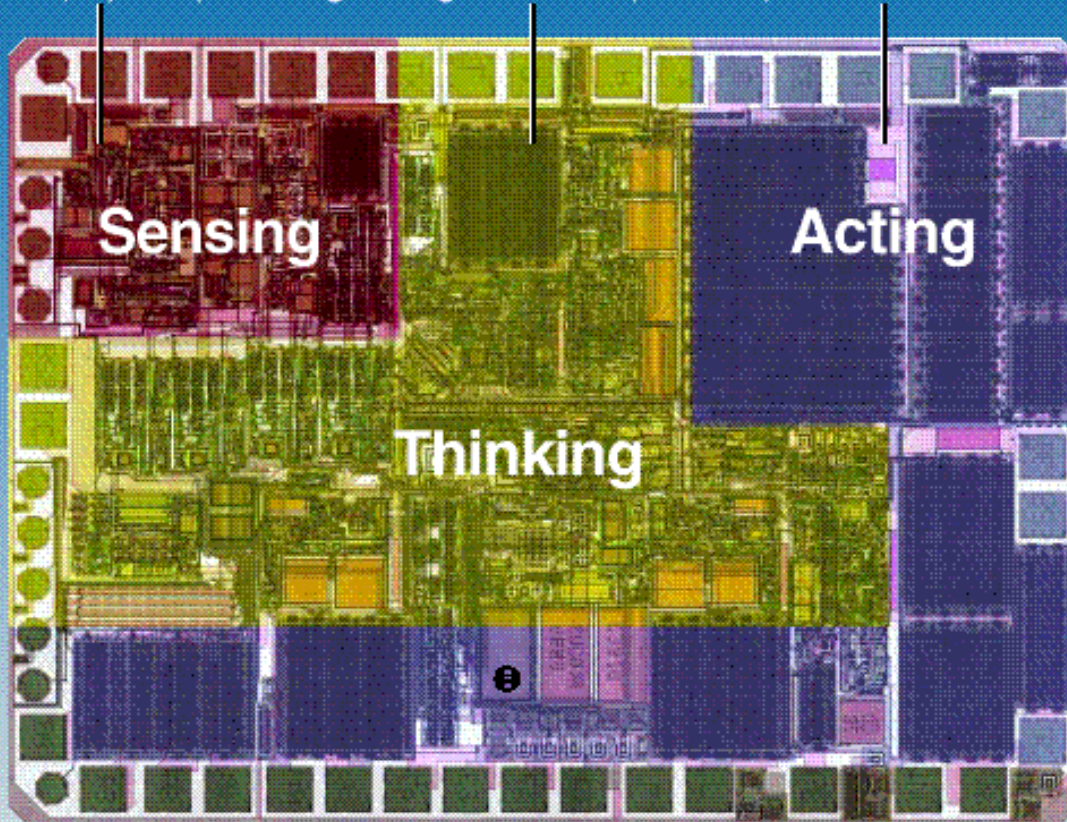




Analog circuits (Bipolar)

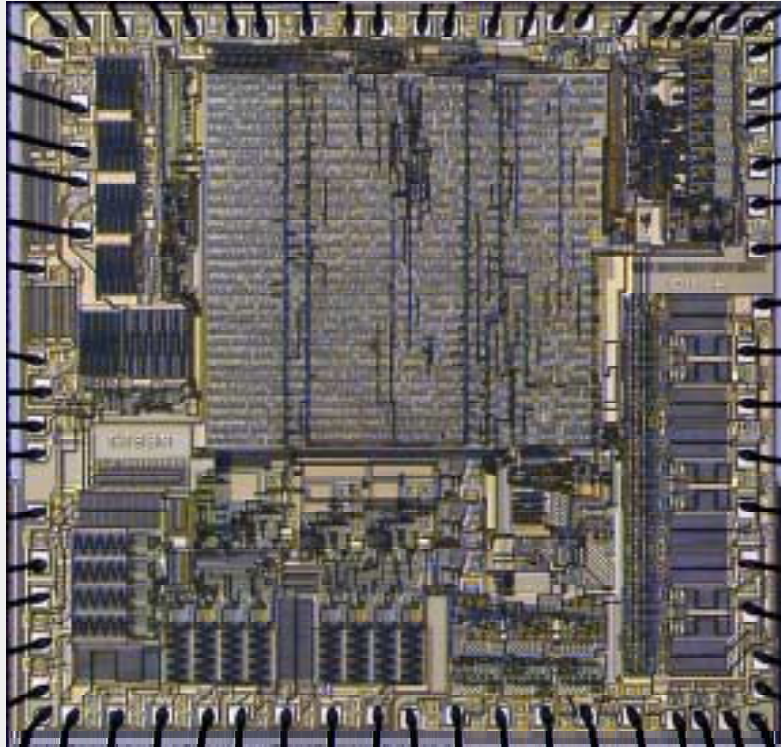
Digital logic circuits (CMOS)

Power circuits (DMOS)





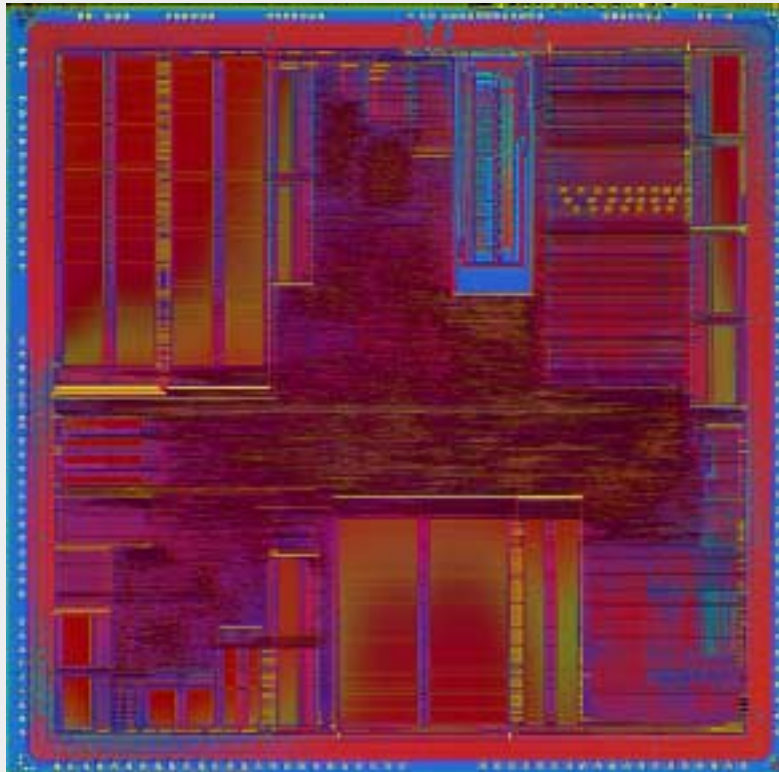
Control unit for fuel injection



Chip size	35 mm ²
Number of components:	23 440
Process:	BCD3
	mixed process



DAB-Fully Integrated Receiver Engine



Chip size: 81mm²

Number of components: **7.9 Mio**

Function: DAB and FM on-chip

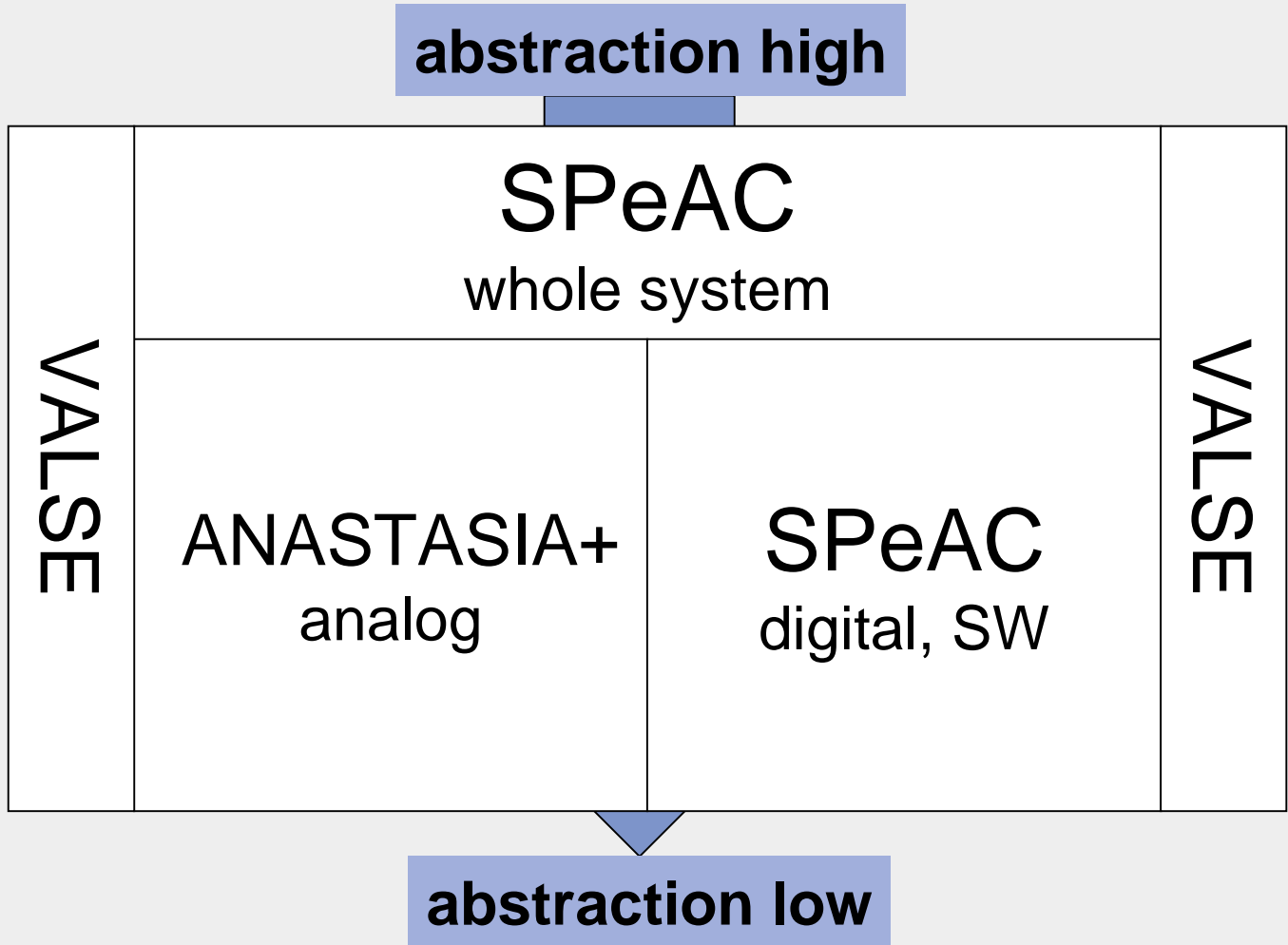
Process: 0.25μm, CMOS



- Development and establishing of a digital system level design flow
- Closing the gap between specification and existing flows
- Better communication between ASIC designers and system designers
- Earlier detection of errors and misunderstanding
- More automation
- Better testability over domain borders



- Coordination at dept. AE/DIC (A. Reutter)
- Subcontractors
 - Investigation tasks
 - Market overview
- Designers as active partners
 - Real world examples from involved departments
 - Correspondent for subcontractors
- PhD student
- Trainees, graduands
- AE/DIC staff





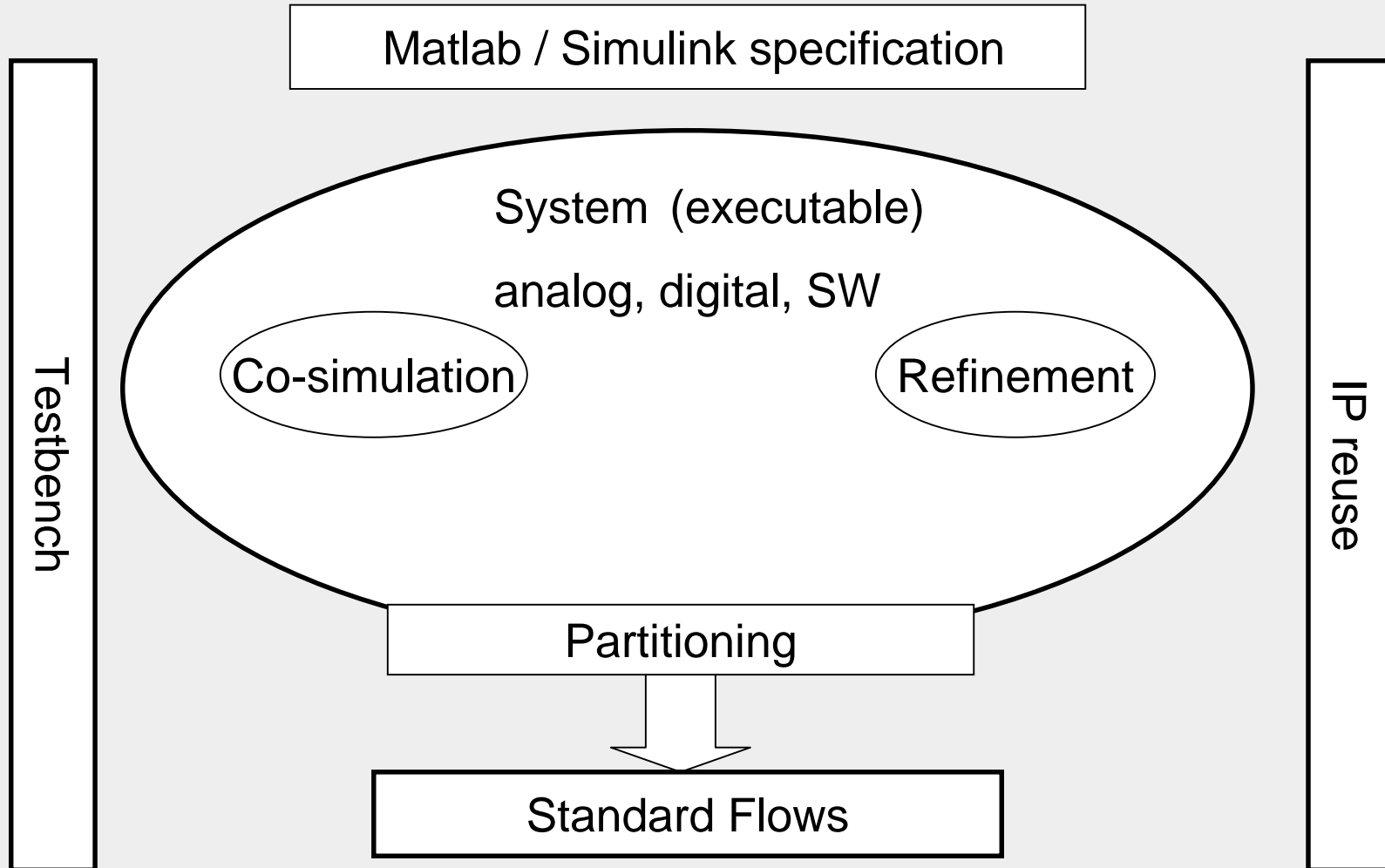
- Co-Simulation of system model and implemented parts (e.g. Simulink - VHDL simulator)
 - uniform description of all components at highest level
 - simulation over domain borders
 - simulation over abstraction levels
- Reuse of testbenches generated for system level model
 - complete verification environment over different abstraction levels
- Automatic VHDL generation from system level description
 - long term goal
 - „correctness by construction“

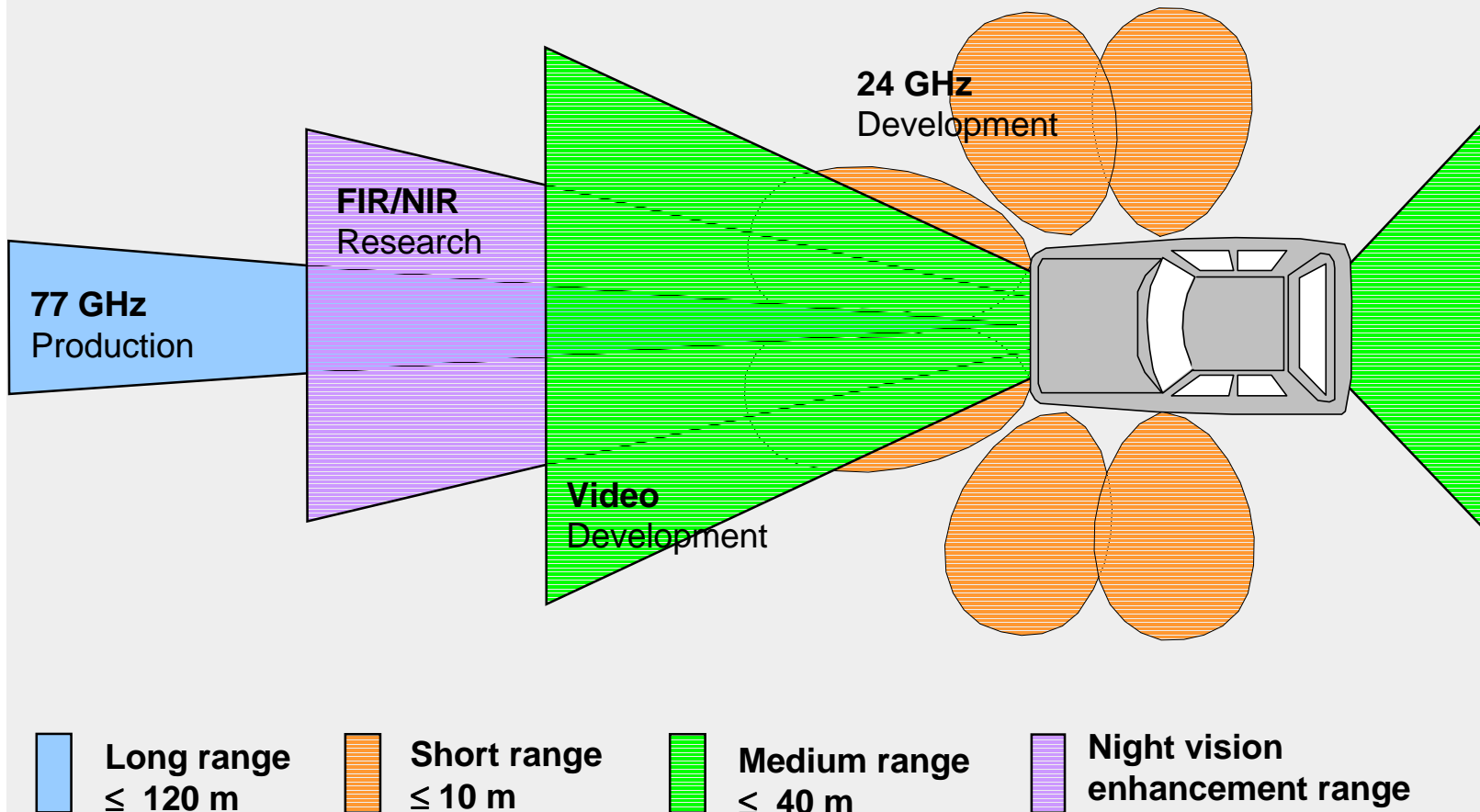


- Investigation of languages for system level design
 - Theoretical concepts
 - Modeling of examples achieved from design departments
 - Subset for synthesis
 - options for design reuse
- Investigation of tools for system level design
 - usability
 - performance, stability
 - synthesis of modeled examples



- Elaboration of possible flow(s)
 - direct compilation from digital modules to VHDL
 - compilation of modules into an intermediate format like C-based languages
- Alternatives for co-simulation (e.g. Simulink-VHDL simulator)
 - Direct coupling: Simulink-Modelsim
 - Own master application which manages the simulators (e.g. SystemC application)
 - HW description with C derivate in RTL style
- Cooperation with The MathWorks
 - support from MathWorks developer
 - information exchange

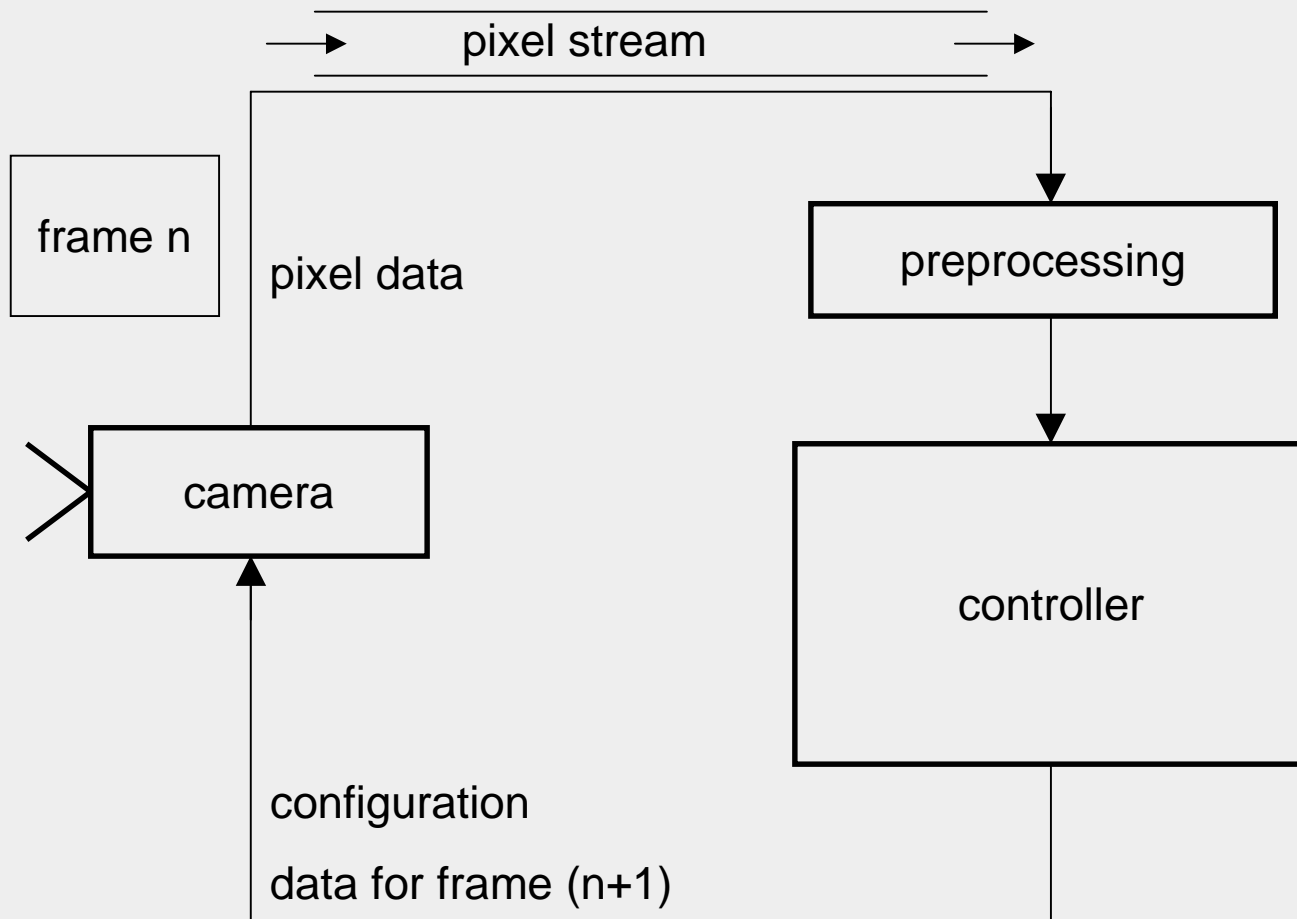






Working example: camera exposure control unit

BOSCH





- System example
 - not only digital HW, but:
 - Different domains: HW, SW
 - Not too complex
 - Availability of
 - ◆ Matlab model
 - ◆ C model untimed / timed
 - ◆ C model bit accurate
 - ◆ VHDL model / C model
- Prototype for the extension of digital flow



- Summary
 - Investigation of languages and tools
 - Elaboration of a prototypical flow
 - Evaluation of this flow with our example
 - Setup of a Simulink-VHDL cosimulation environment started:
- Next Steps
 - Establish a co-simulation environment
 - Elaboration of a testbench concept