MEDEA+
FLEUR/SPEAC
Workshop

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GOALS on FLEUR

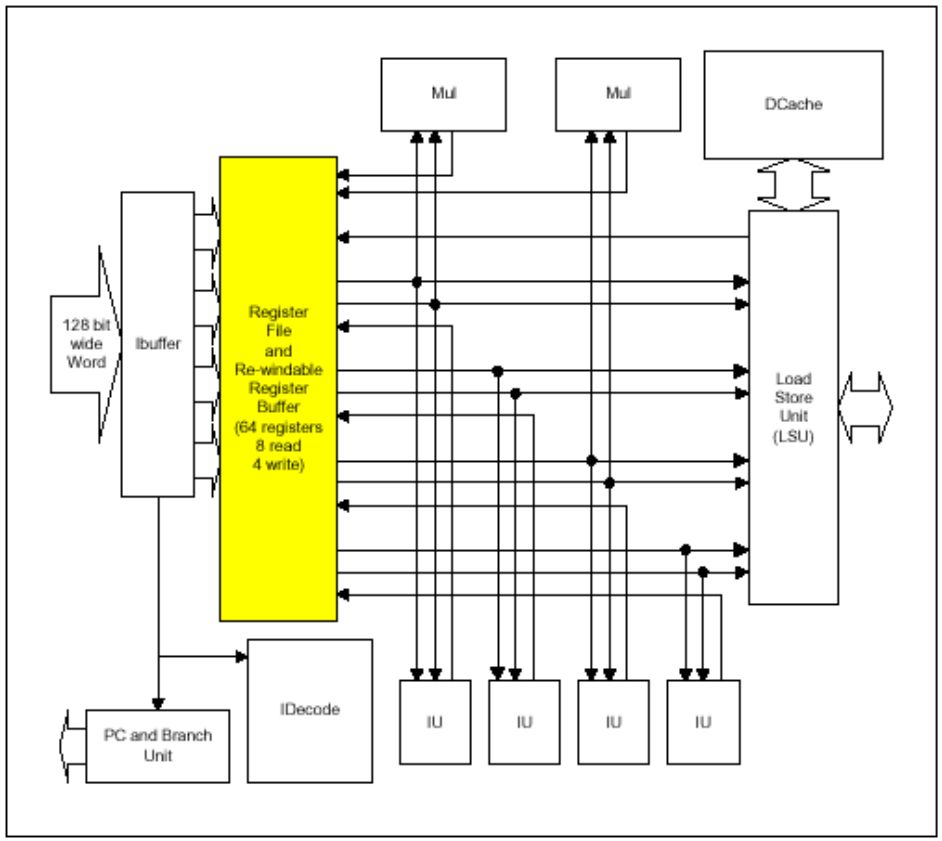
- Provide an integrated methodology for the power estimation and optimization of HW/SW systems at the highest abstraction levels.
- Widely explore different design alternatives in the architectural design space
- Define power optimization criteria for the compilation phase of SW code for VLIW architectures.
- Tune the target system architecture aiming at performance and power optimization

WP1: Heterogeneous System Design

- **Main Goal**
  - ***Collect design practices from system houses***
- **Task RI 1.1**
  - Assessing the system design methodology exploited in ST
- Ultra low power VLIW processor. Wide range attack:
  - Power driven SW optimization
  - Architecture and micro-architecture definition
  - RTL implementation
  - Low Leakage circuit design
  - Highly optimized cache memory design
  - Process and Technology
- **Deliverable**:
  Lx design and architecture specification doc

Target System Architecture

- Lx processor: 128 bit VLIW architecture
  - statically scheduled VLIW multi-cluster
    - Four parallel issues, in-order 6 stages pipeline
    - Four 32-bit integer ALUs Two 16x32 MULTs
    - LOAD/STORE unit and branch unit
    - RegisterFile (8R,4W)
    - I and D-cache



WP2: Innovative Design Methodology workpackage leader: ST

- **Main Goal**

  To build a new design methodology for complex SoC, based on state-of-the-art tools and best practices coming from other industrial fields and EDA providers.

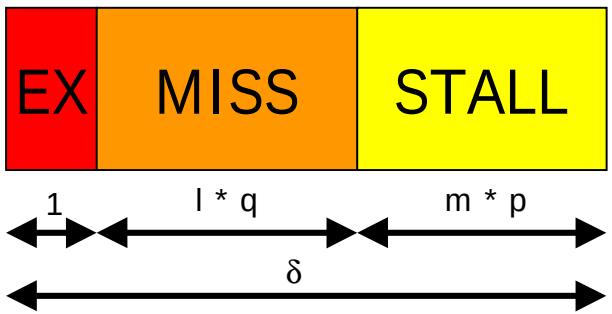
WP2: Innovative Design Methodology

- **ST's main objective**
  - **Define a thorough methodology for low power design at the system level**
- **Task RI 2.1**
  - **Definition of an effective metrics to evaluate the power/speed trade-off among etherogeneous system architectures**

- **Deliverable:**
  Power metrics across the Design Chain doc

WP2: Innovative Design Methodology

- **Task RI 2.3**
  - **System level power estimation and exploration for high-end processors**
  - **Including dynamic power profiling, memory hierarchy optimization, system buses power analysis and micro-architecture design**

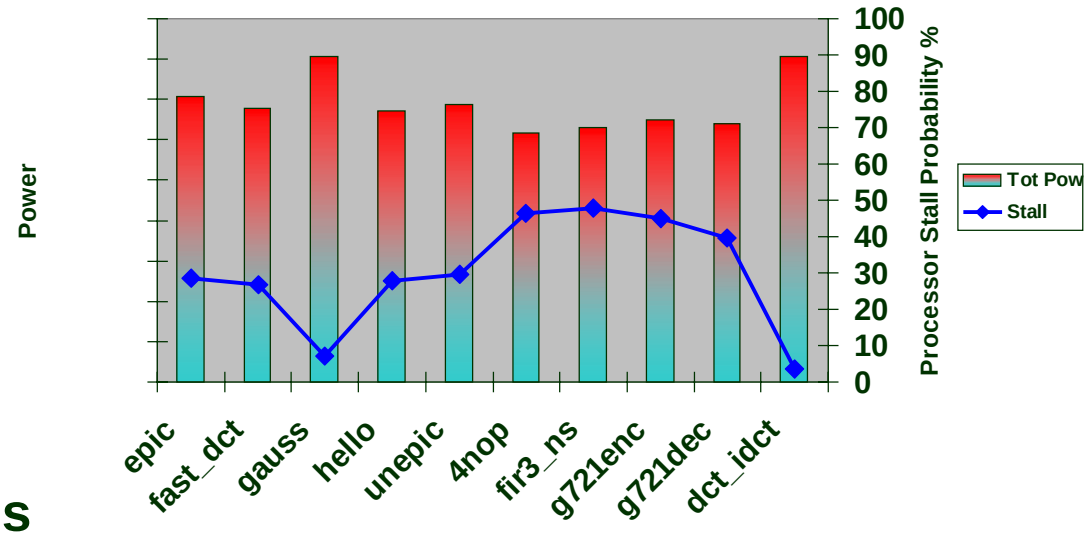


Cycle based execution of
a bundle of parallel instructions

- **Deliverables**
  - **Power/Speed design exploration of the processor to storage sub-system doc**
  - **Power macro-modeling and estimation of system buses doc**

WP2: Innovative Design Methodology

- **Task RI 2.4**
  - Exploiting the power exploration methodology to the design of an ultra low power processor architecture targeting the mobile multi-media terminal: Lx VLIW



- **Deliverables**
  - Lx power profiling and estimation doc
  - Architectural exploration based on a extensive set of multi-media application benchmarks

WP3: *Requirements for Next Generation SoC Design*

- **Main Goal**
  - ***to define the next generation toolset required for the design of future SoC's***
- **ST's main objective**
  - **Define an advanced design environment for power/performance exploration of future processors**
- **Task RI 3.1**
  - **Parametrizing the IL power model of Lx in order to address multi-cluster computing systems (i.e.: massive parallism)**
- **Deliverables:**
  Parametric characterization and modeling of high performance cace memories in deep sub-micron tech
- **Multi cluster power modeling and estimation for both HW and SW profiling doc**

WP3: *Requirements for Next Generation SoC Design*

- **Task RI 3.2**
  - **Identification of the most effective power estimation methodology for system buses and integration into the low-power system design framework**

- **Deliverables:**
  System buses communication tracing and stat's profiling in order to identify the optimal bus encoding techniques doc

- **Integration of what above into the low-power system design framework**