MESA

Multi-processor Embedded Systems Architectures

Project Highlights

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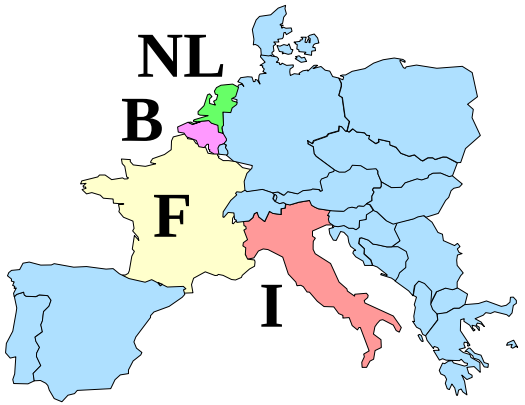
MESA Project : identity card



- Name
  - *Multi-Processor Embedded Systems Architectures*
- Key data
  - 2001-2004, 400 man.year, 21 partners, 4 countries
- Partners :
  - **SMEs** : ACE, ARM, CAPS, CoWAre, MetaSymbiose, PolySpace, TCT
  - **Industrial** : Alcatel-Bell, Bull, EADS-Telecom, Philips, ST (Project Manager)
  - **Labs & institutes** : INRIA, IMEC, Universities of Grenoble (TIMA), Leuven (KUL), Nantes (EPUN) and Paris (LIP6)
- Goals :
  - Developing open system-level design flows, from specifications to HDL or C
  - Exercizing them on real test-cases (e.g. webcam, MP3 player, wireless…)
- Structure :
  - 1. Domain analysis
  - 2. Multi-processor architecture
  - 3. Codesign & communication
  - 4. System validation

- **Global goals and organization**
- **Global achievements**
- **3 examples**
- **Annex: detailed list of outcomes**

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Problems to solve in MESA

Approach	Dangers	Design challenges	Solutions worked-on in MESA
Technical advance	Under-exploit new silicon techno-logies	Higher **complexity** on the same chip	Matlab models, Transaction Level Models
		IC speed, area & power	SPIN network, precompiler, low-power methodology, memory footprint reduction
Reactivity	Missing the time-windows to reach market	Reduced **time-to-market**	Methodology for designing DSP cores, cosimulation platforms
		Make it right **at first time**	Symbolic simulations, validation platform, model checker, validation of cores, code validation
Flexibility	Mono-application solutions	Easier **consolidation of specs**	Application analysis, executable specifications
		Possibility to choose different **trade-offs**	Architecture exploration

Complementarity with SPEAC

WP1-Domain Analysis & Modeling

Communication, Multimedia DSP, Multi-computing System

C, SystemC, UML, XML

WP2-Multiprocessor Architectures

C-RISP processor, SPIN-Network, SVM multi-computing architectures

WP3-CoDesign and Re-configurability

Architecture Exploration&Synthesis, SystemC Design flow, Sw optimization & compilation

WP4-System Validation

Formal Verification, System Prototyping, Sw Simulation/Debugging

MESA

WP1-Application & Demonstrators

Automotive, Avionic, Communication

WP2-System Specification

Java, C++, Matlab, SDL, SystemC, HDLs

WP3-Algorithm/Architecture Co-Design

Architecture evaluation, System IP-design

WP4-Hw/Sw Co-Design and Communication Layers

Generation of real time OS, Interface wrapping

WP5-Architecture Assessment

Co-Simulation, System Prototyping

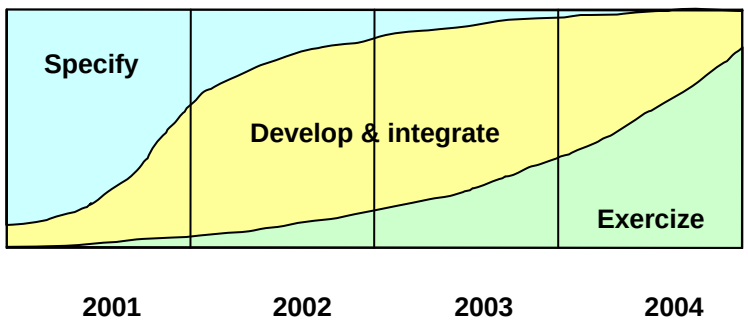
WP6-Heterogeneous Systems

WP7-Configurable Design flows

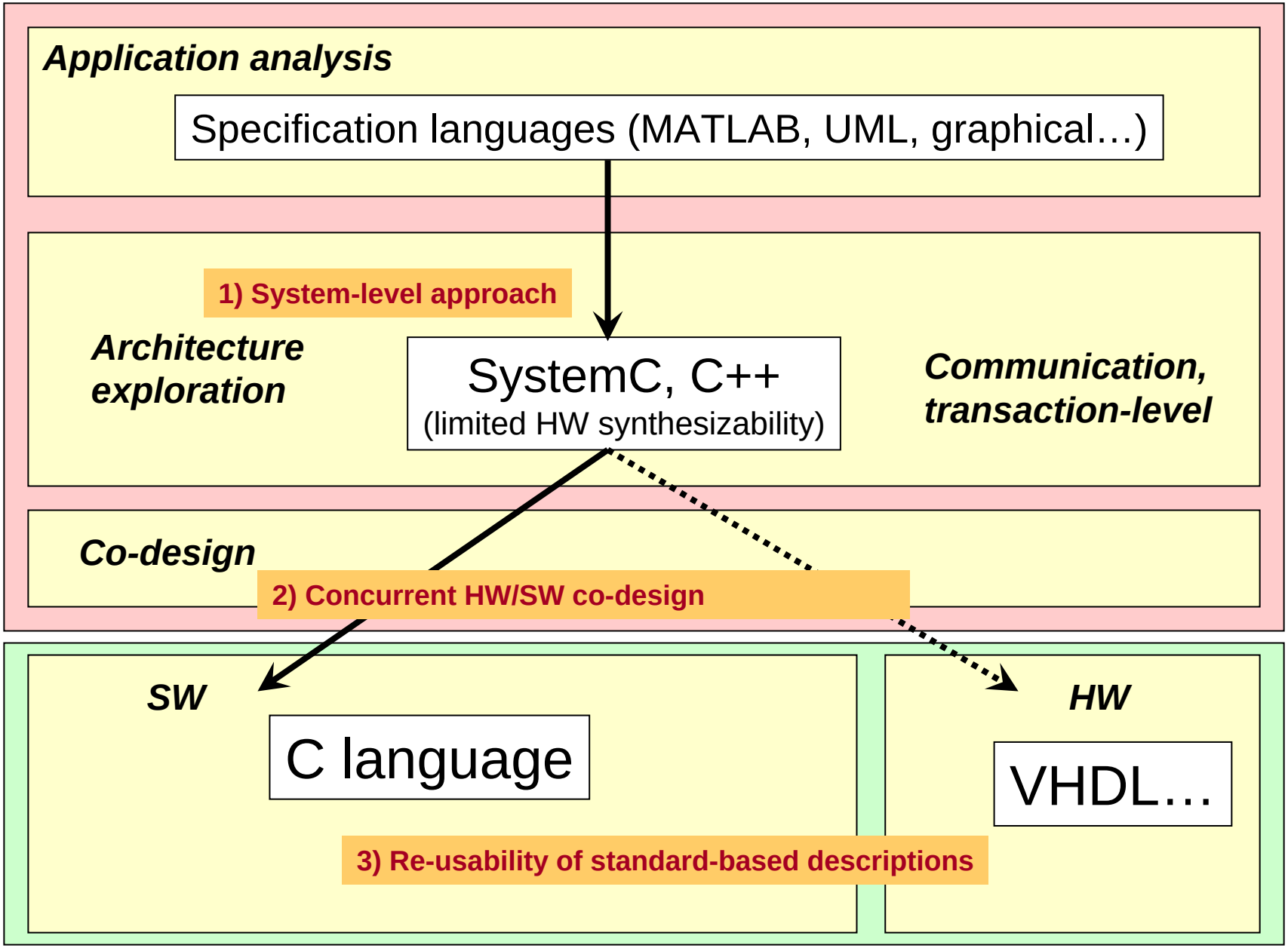
SpeAc

MESA Project : synergy, outcomes

Test-cases ⟷		Tools	
Provider	**Type**	**Provider**	**Type**
Philips	Video MPEG4 MP3	IMEC TCT	DTSE Chess-Checker
ST	Face recognition	Coware	N2C
EADS	Digital radio	ARM	ART Designer
ST	Audio-video	ACE	Compiler
Bull	Multi-computing	Meta-Symbiose	Logan
ST	Cache controller, DSP operators	TIMA	Formal verif. with symbolic simulation



Open MESA top-down system level design solution



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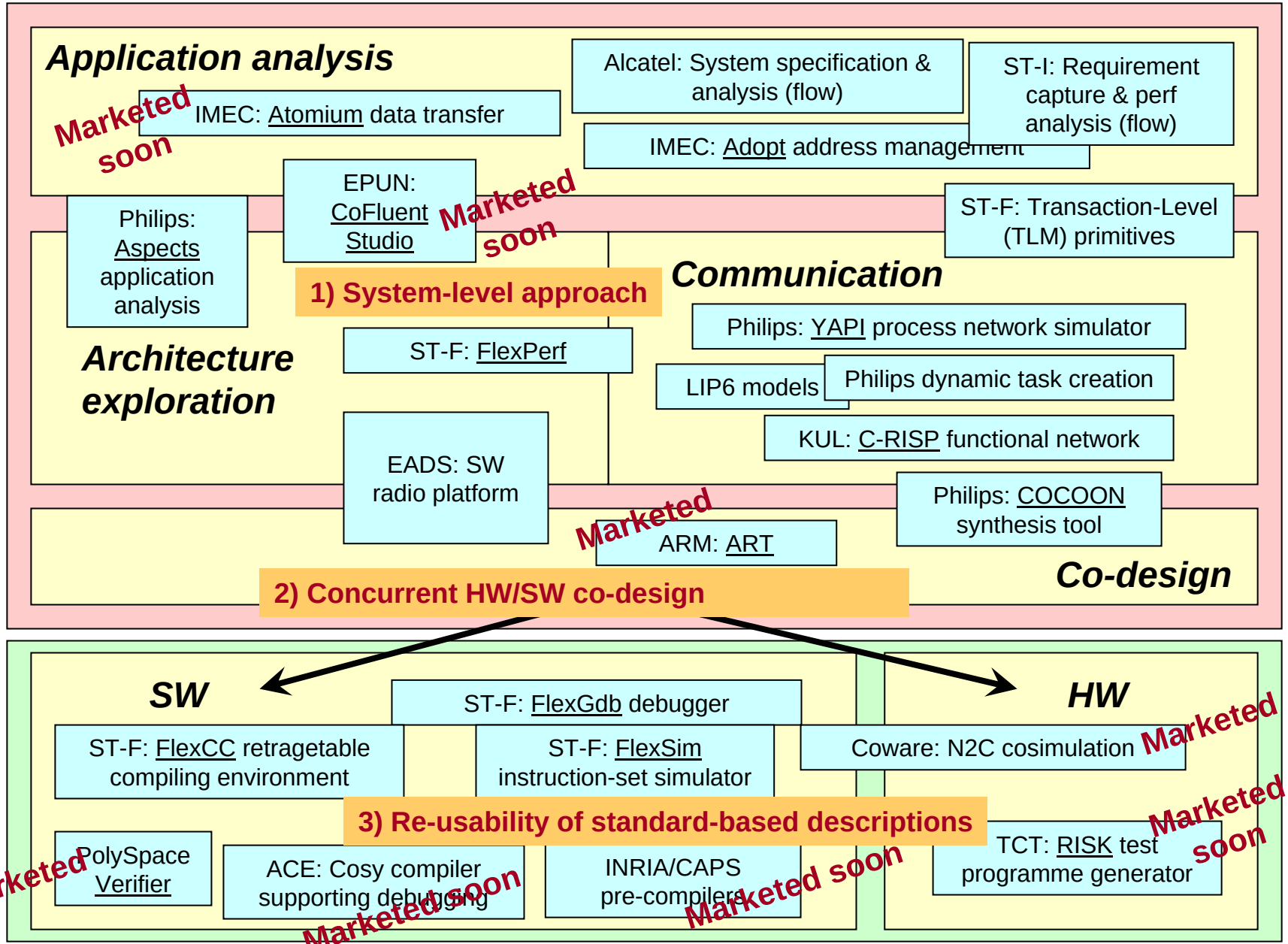
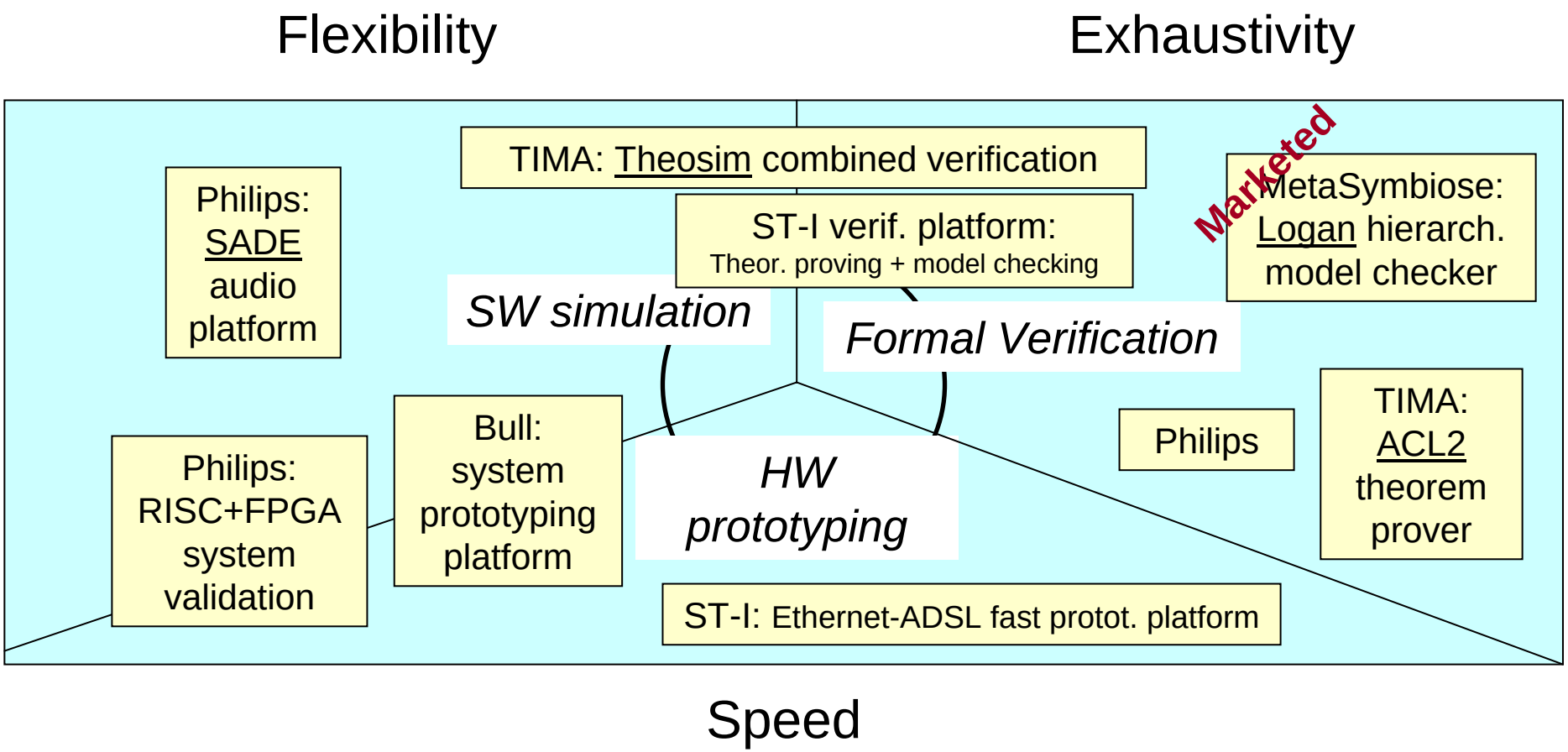
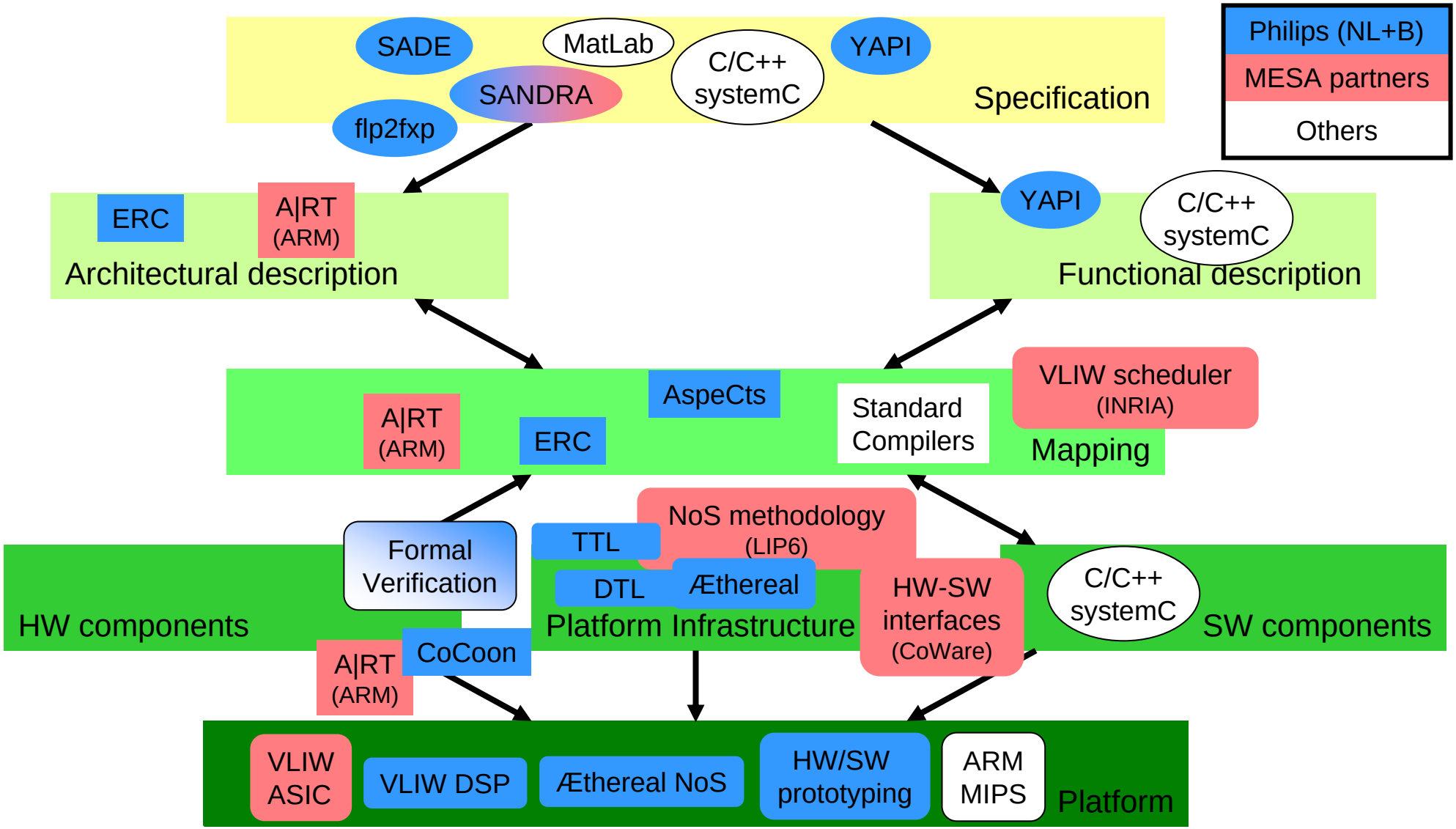


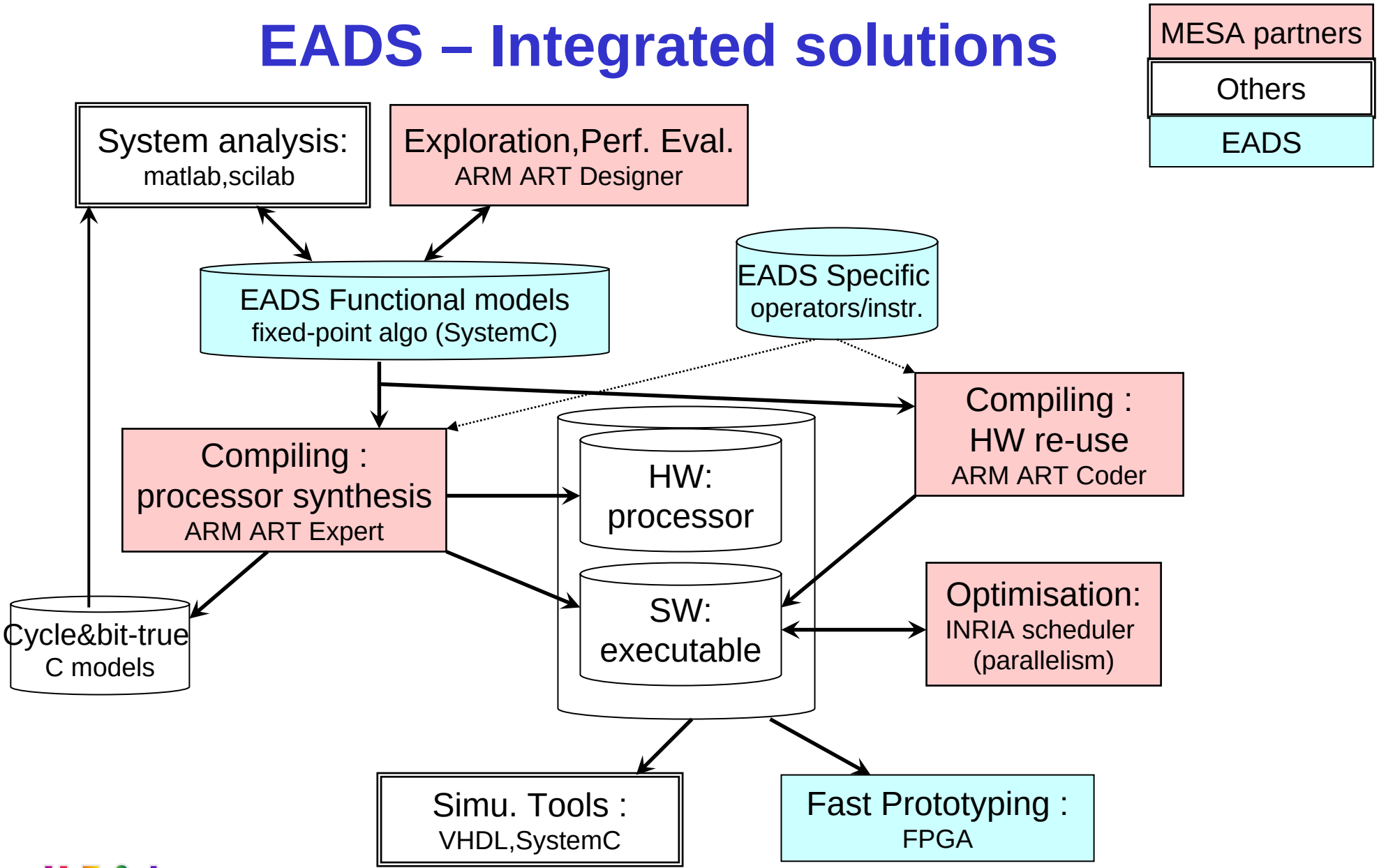
MESA Sytem-level Verification Solutions



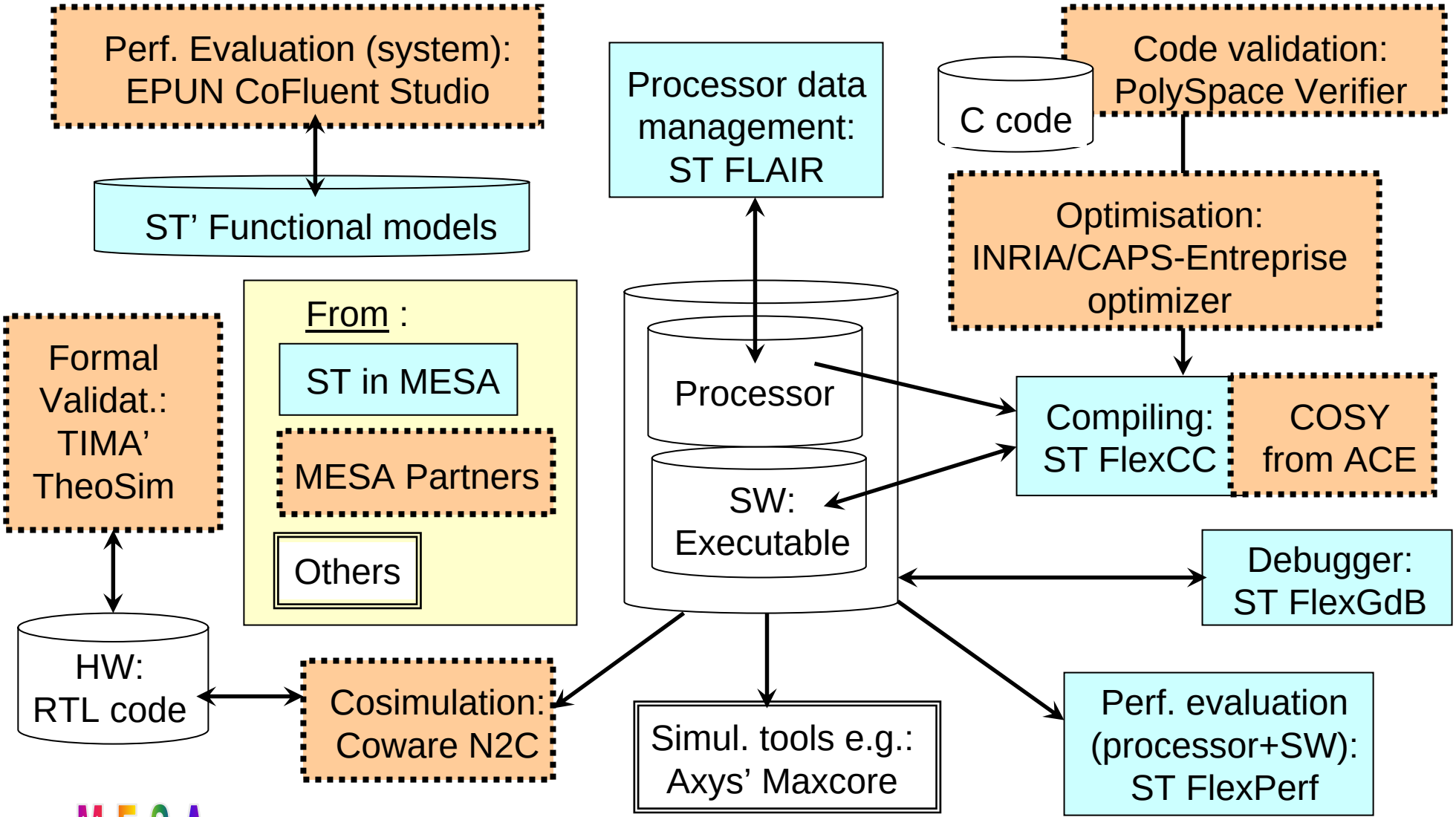
Philips – Integrated solutions



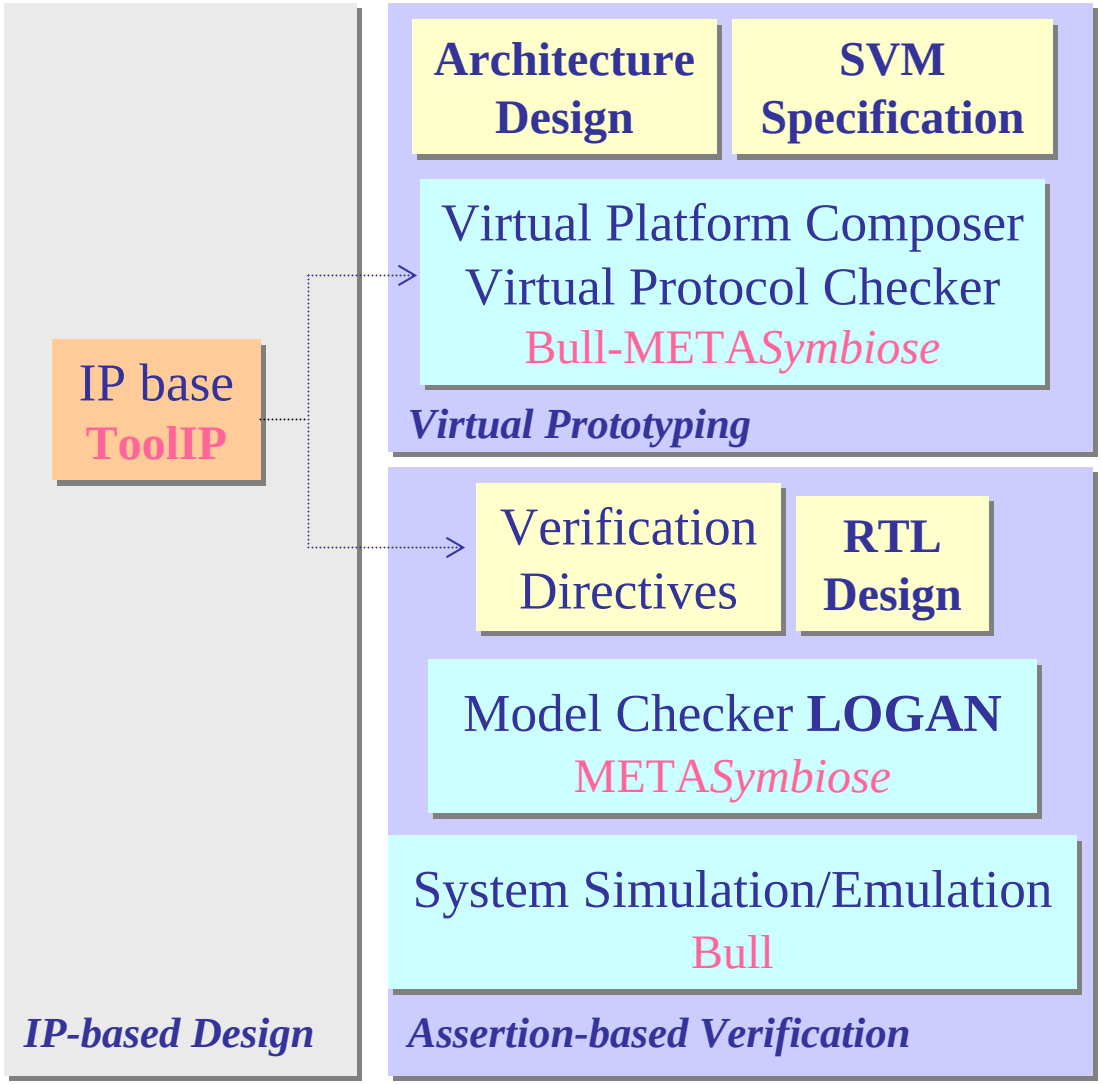
EADS – Integrated solutions



ST – Integrated solutions



Bull – Integrated solutions



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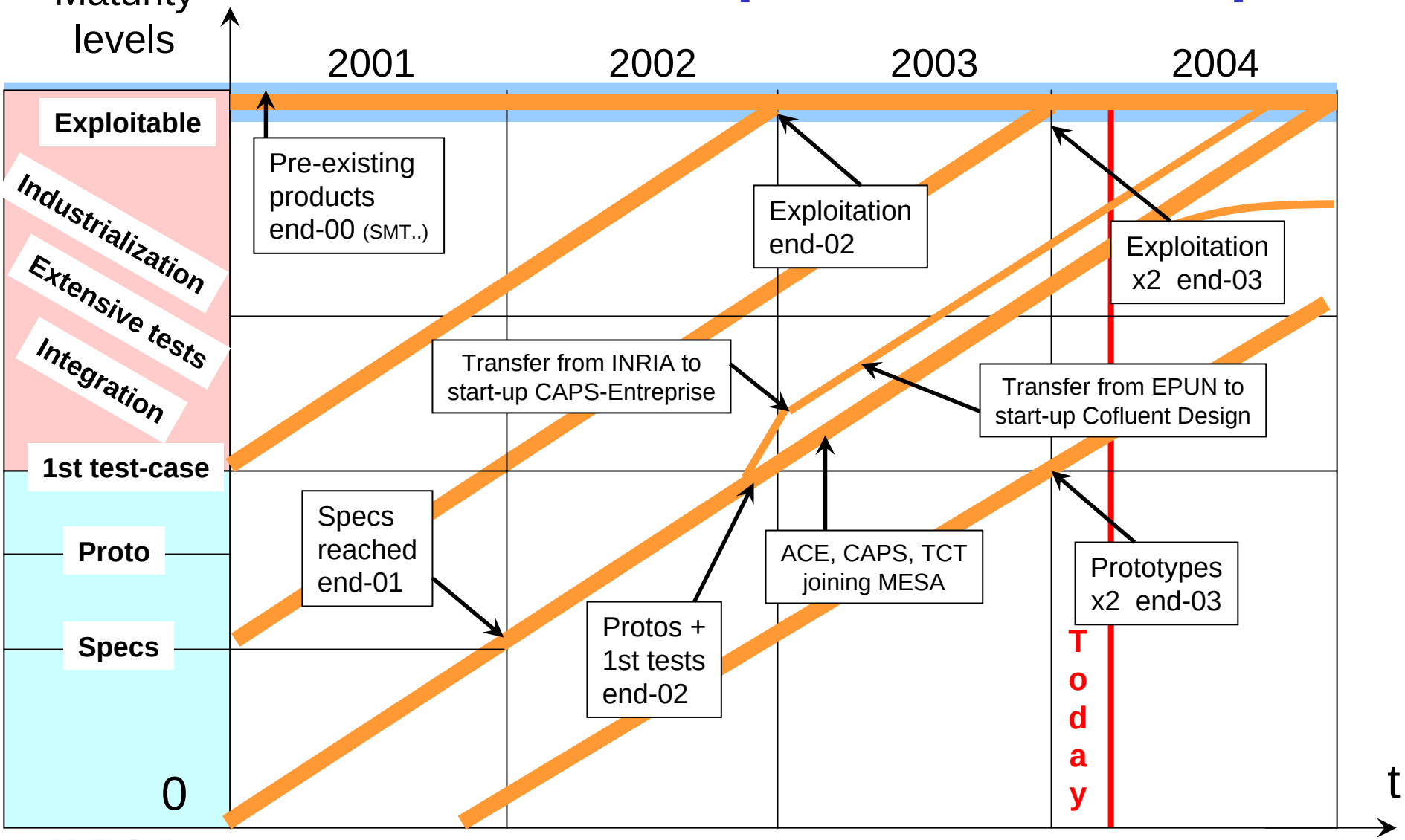
MESA developments road-map



Metrics (1)

WP	Partner	Metrics
Design manpower - Design speed - Time-to-market		
1	Philips	SANDRA allowed 5-10 fold reduction in programming effort
1	Philips	Automated optimization of task concurrency management allows 40% gain of design time **New 2003**
2	LIP6	Simulation speed-up of a factor 7 with model of complete SPIN network
2	Coware	10x faster simulation, 10x faster compilation over RTC
3	ST	FlexCC2 compiler performance X 3 with equivalent code size; time saving in application development : 66 %
4	Philips	HW/SW prototyping of error corrections : 2-3 times faster, cost divided by 4
Silicon area		
1	IMEC	ADSL manual experiment, footprint -33%

Metrics (2)

WP	Partner	Metrics
Power consumption		
2	Alcatel	25% reduction in power consumption
3	Philips	Energy gain by a factor of 10 compared to sequential ARM processor
IC execution speed - Simulation accuracy		
1	IMEC	ADOPT allows 25-75% speedup, depending on CPU, compiler, application **New 2003**
1	Philips	Automated optimization of task concurrency management allows 50% gain in cycle optimization **New 2003**
3	INRIA	Global code compression can reach 25%, depending on appli. **New 2003**
3	Philips	Combining speed & power, COCOON beats existing DSPs
3	Philips	Reconfigurable co-processors are x100 faster for computation-intensive kernels
4	Philips	Accuracy of Trimedia simulator is moving from 10-20% to 5% **New 2003**
4	ST	HW prototyping (Aptix) of MultimediaCard (MP3 player) runs at 20 MHz **New 2003**

2 new start-ups

- From INRIA (Nat. Computer Sciences Institute, Rennes):
  CAPS Entreprise (Rennes)
  on C optimizer with multimedia instructions
- From EPUN (University of Nantes) :
  CoFluent Design (Nantes)
  on Architecture modeling and performance evaluation

Cofluent was awarded in 2003 the *Tremplin Entreprises* price by French Ministry of Research
Mrs Claudie Haigneré & President of Senate Mr Christian Poncelet

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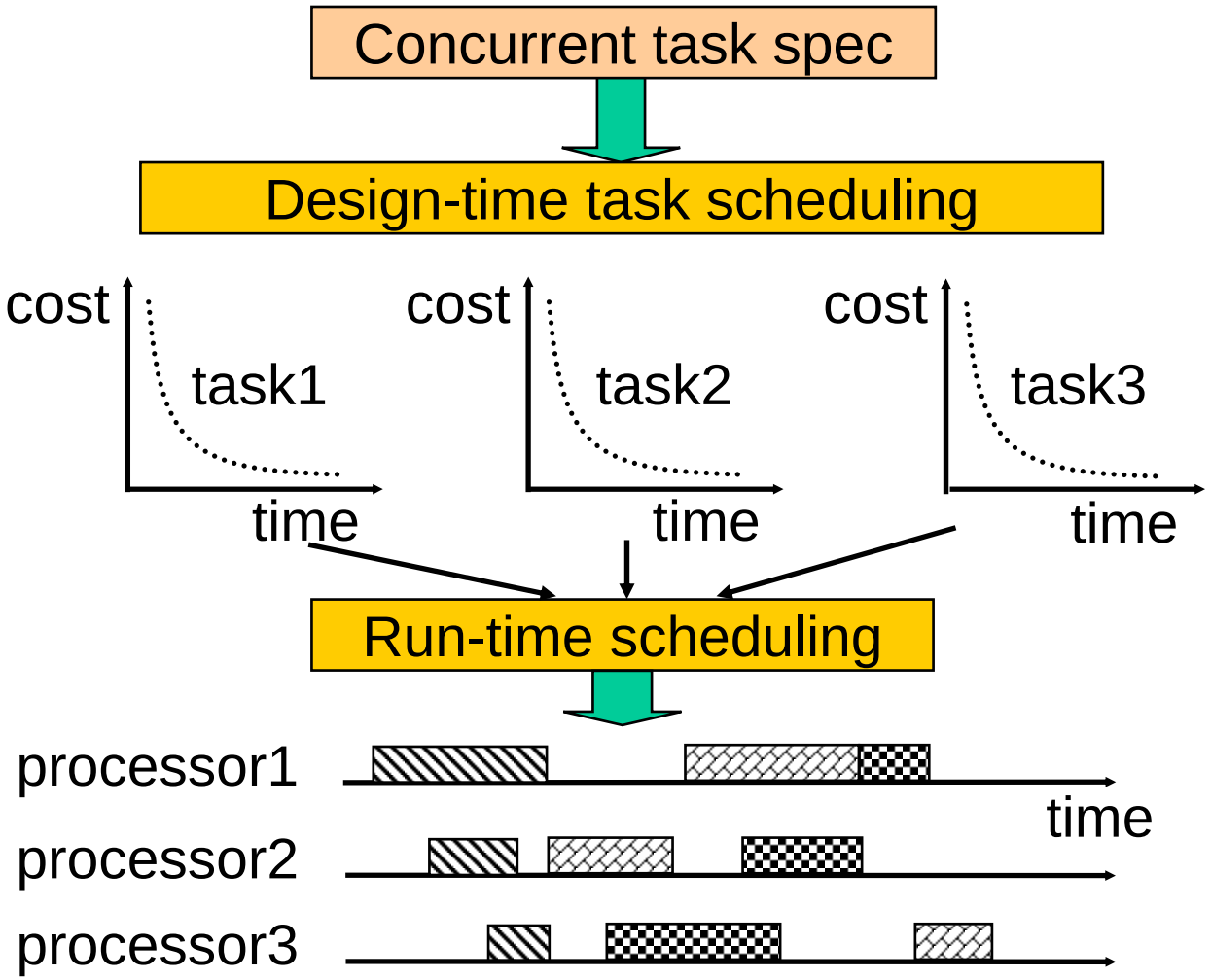
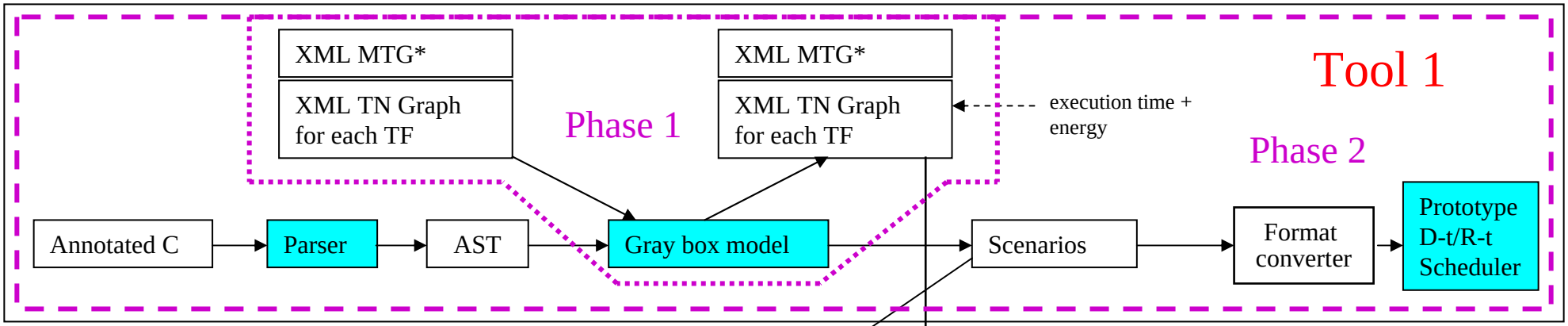
Example #1: IMEC (coop. with Philips, Coware…)

- Applications, test/cases
  - **Applications handling large amount of data, e.g. communication & multimedia**
- Challenges
  - **Memory synthesis and mapping: optimization of area, throughput and power consumption**
- Tools & methods
  - SBO: Storage bandwidth optimization (parallel access to meet timings)
  - MA: Memory allocation (memory architecture wrt area & power)
  - ADOPT: In-place optimization (address mapping)
- Results
  - 25-75% speed-up with ADOPT, footprint reduction reaching -33%

Task Concurrency Management: design flow (IMEC)

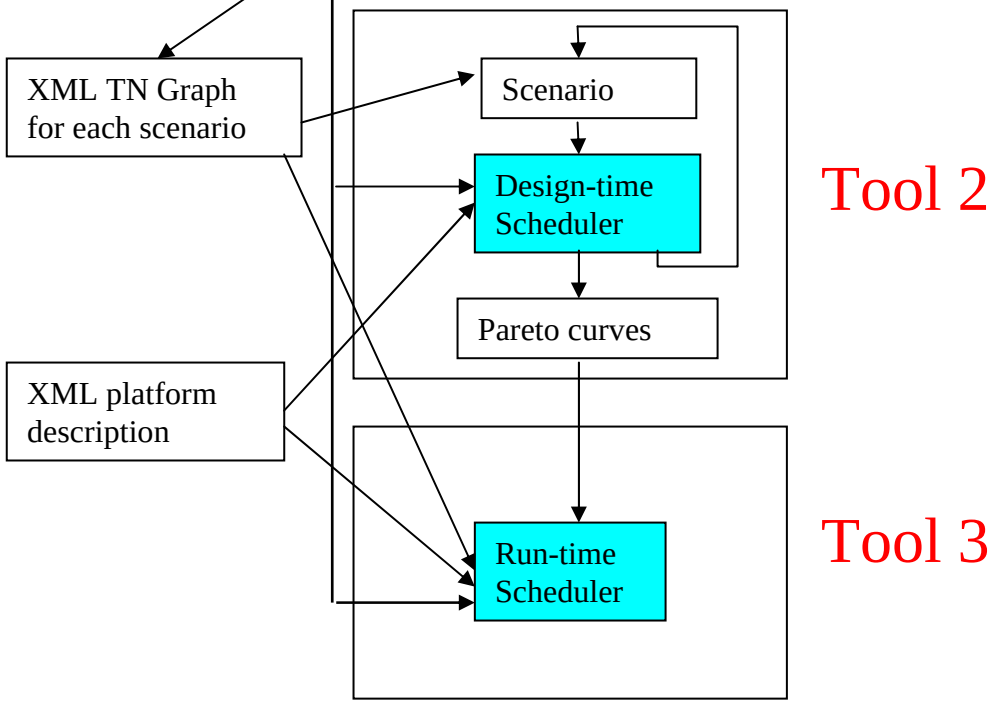


Task Concurrency Management: tool flow (IMEC)



- ✓Graybox model classes (done)
- ✓Parser/AST interfacing (done)
- ✓ Graybox<>XML (done)
- ✓ AST>Graybox extractor (done)
- ✓ Scenario creation (done)
- • Interface PhD tool (Q4/03)
- • Evaluate PhD tool (Q4/03)

- ➢ Design-time scheduler (2004)
- ➢ Run-time scheduler (2004)
- ➢ DEMO: 3D application (2004)



Memory Synthesis activities (IMEC)

- 06/03 Evaluation report on ADOPT address optimization
  - Speedup 25..75% = function(cpu, compiler, application)
- 12/03 Optimization prototype for arithmetic expressions (RACE)
- 12/03 Integrated SBO and MAA prototype
  - First version of automatic allocation implemented
  - Integration SBO/MAA started, expected to be on-time
- 06/03 Methods for Memory Hierarchy exploration/optimization
  - on-time
- 12/03 Techniques for Data Reuse exploration/optimization
- 06/04 Techniques for Memory Hierarchy Layer Assignment
- 12/04 Prototype for Memory Hierarchy Layer Assignment

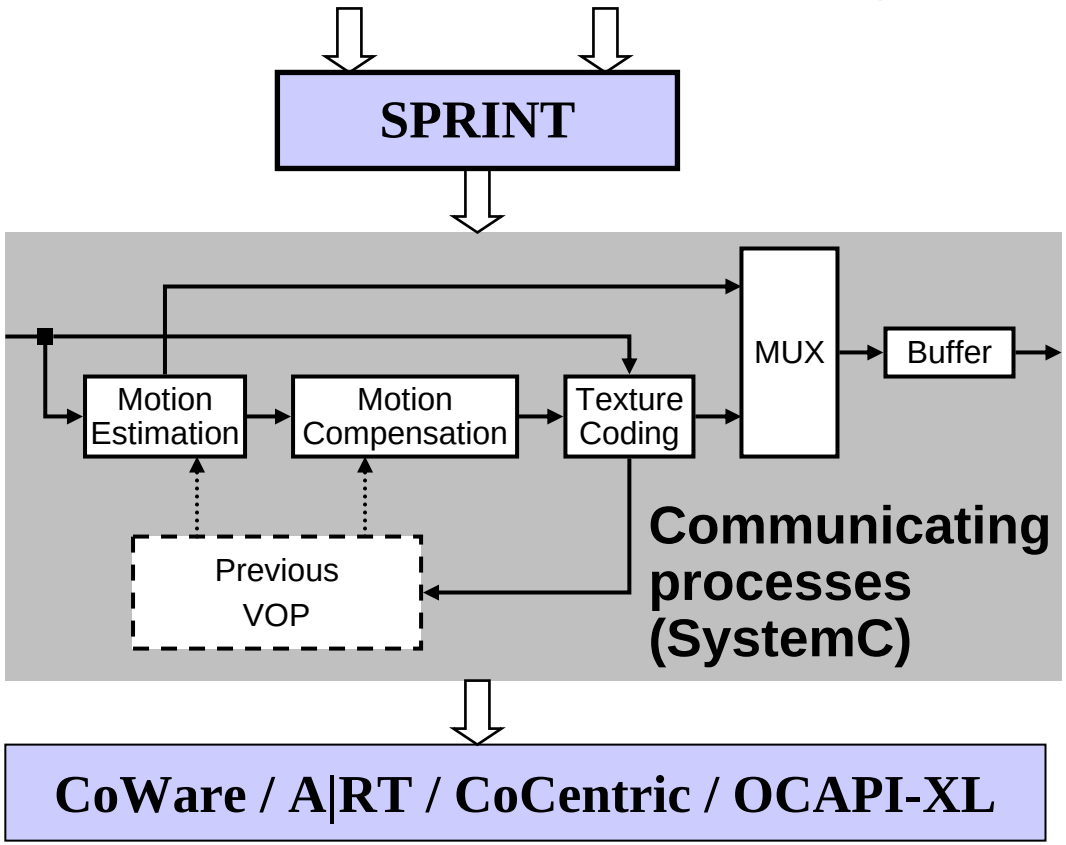
Coupling to existing design environments (IMEC)
SPRINT: from sequential code to parallel tasks

```
int main(int argc, char *argv[])
{
  char control_file[100];
  int rc_type;
  VO *vo_list = 0;
  ...
}
```

C code

```
shared_variable(Previous_VOP);
make_process(Motion_Estimation);
make_process(Motion_Compensation)
;
make_process(Texture_Coding);
...
```

Pragmas



- 06/03 User requirements
  - coding started
  - basic functionality 12/03
  - … testing + improving
- 06/04 Basic SPRINT prototype
- 12/04 Evaluation report of Basic Sprint prototype

Example #2: ST & EPUN

- Applications / test-cases
  - **MPEG4 encoder-decoder**
- Challenges
  - **Timed system-level modeling & performance evaluation (EPUN). Early functional SW development & efficient simulation speed (ST)**
- Tools & methods
  - SystemC generation & simulation for functional/architectural models (EPUN)
  - Transaction level methodology (TLM) including communication channel
- Results
  - Automatic generation of the architectural model (timed-functional model mapped onto a platform)

Transaction Level models & communication channel (ST)

- Modeling methodology at the transactional level
  - Applied to vanilla models (timer, interrupt controller, …)
  - Experimented on a MPEG4 codec
  - Used by ST division for developing embedded software
- Modeling infrastructure and prototyping activity
  - First version of a Transaction Accurate Communication channel (TAC) completed
  - Upgrades ongoing to support communication model refinement
  - Production version planned for Q4
  - Interactions with EPUN/MCSE for SystemC model generation from MCSE toolbox and discussions around a dynamic profiling tool
  - Joint paper submission to DATE'03

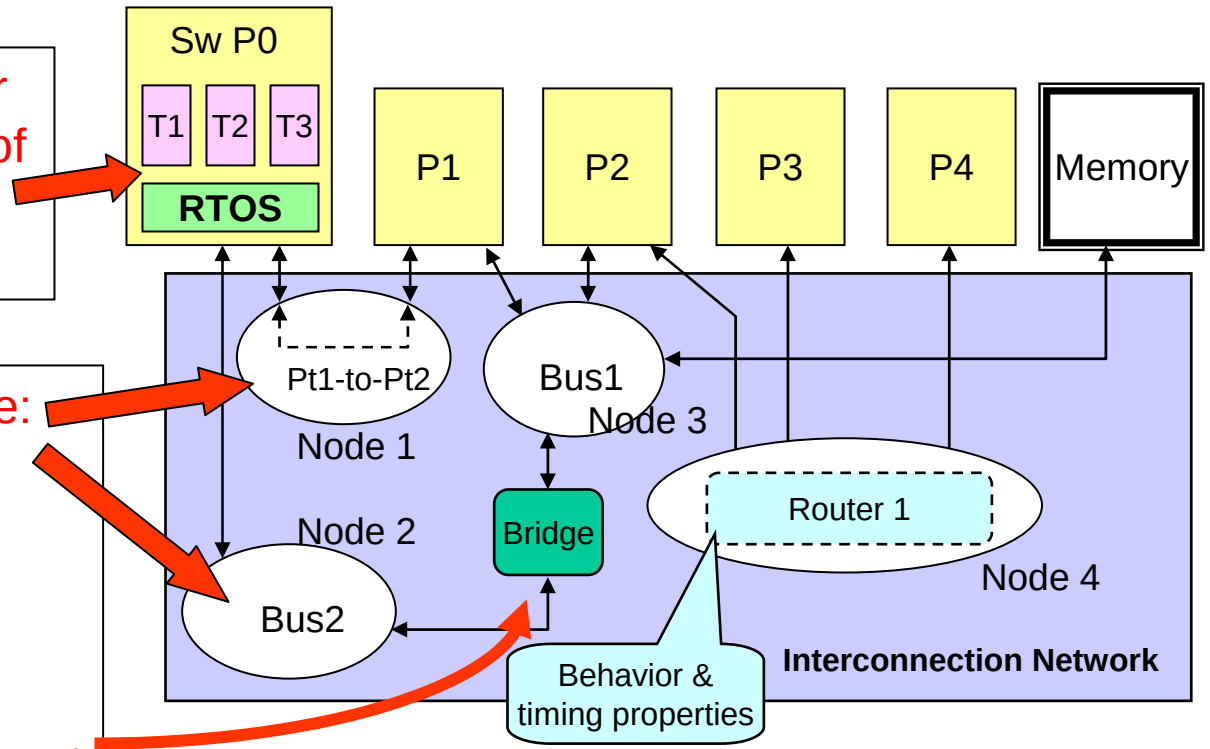
SystemC architectural model (EPUN)

- **Goal in 2003**
  - generation of a SystemC architectural model for Hw/Sw co-simulation
  - enhancement of the communication model for performance evaluation

Simulation of a Sw processor with its links, RTOS, the set of functions and their inter-relations (timed model)

Model selection for each node:
Bus,
full router,
direct point-to-point links
external model

Addition of the bridge component



SystemC architectural model (EPUN)

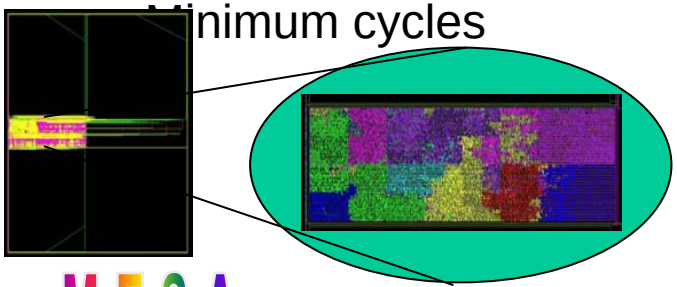
- Model of an abstract RTOS for a Sw processor in SystemC
  - Operational
  - Integration into our tool : automatic generation of the architectural model (timed-functional model mapped onto a platform)
  - Integration of external IP processors under investigation
- Enhancement of the communication network model (NoS)
  - type selection: Bus, full router, direct point-to-point links
  - addition of the Bridge component
  - Operational and integrated into our tool
  - Addition of user-defined models : operational
  - TLM standard for communication model creation under investigation

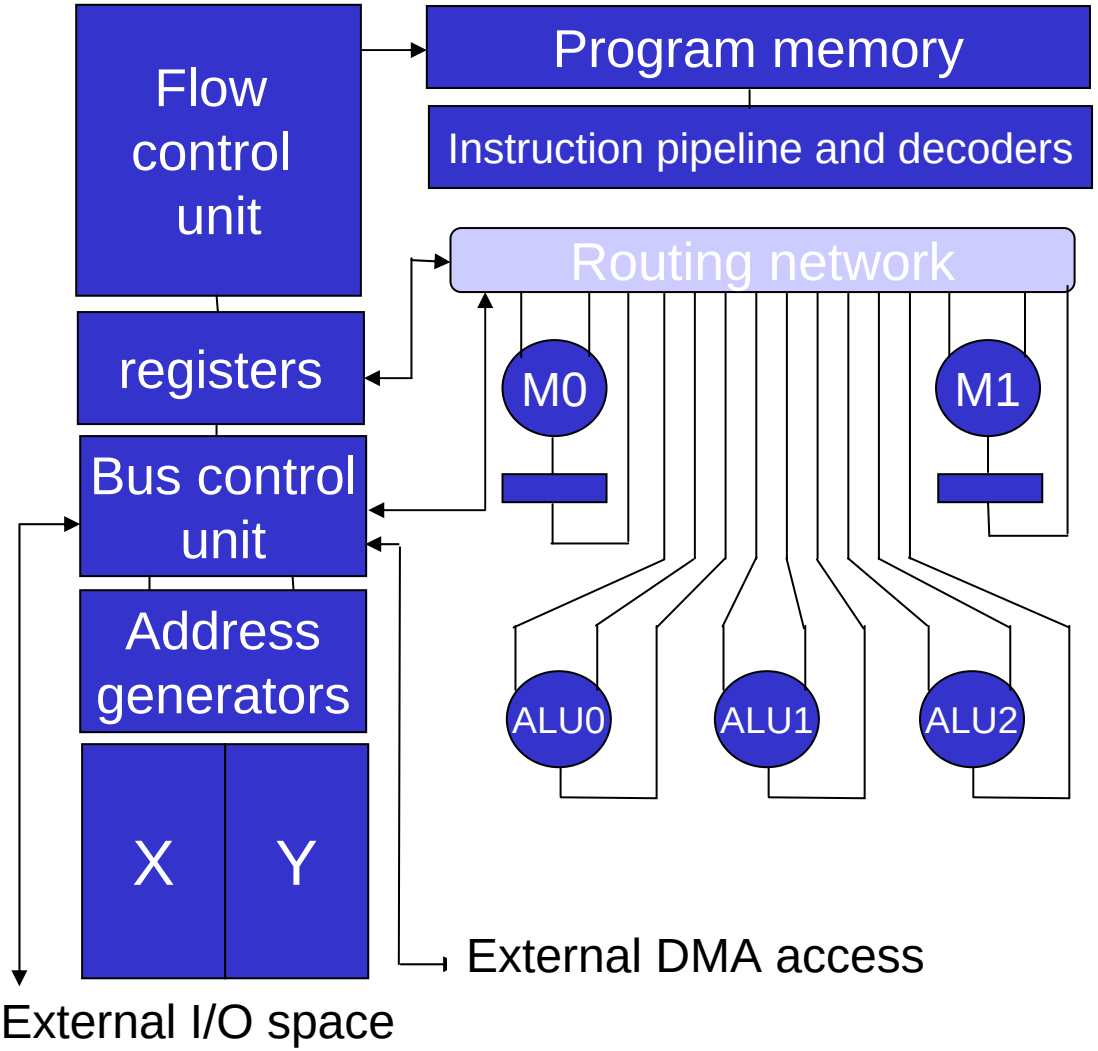
Example #3: Philips & TCT

- Application / test-case
  - **MP3 audio decoding on a DSP core**
- Challenges
  - **Low power, reconfigurability**
- Tools & methods
  - Co-development of core & C-compiler
  - Instruction compaction technique in Chess compiler (TCT)
- Results
  - 25% code size saving
  - MP3 at 1 mW

Processor architecture exploration & optimization (Philips)

- Reconfigurable Ultra Low Power Audio DSP (CoolFlux DSP)
- ULP techniques used throughout complete design hierarchy
- Co-development Core <-> C-compiler
  - Full Exploitation of parallelism
  - Maximum code density
  - Minimum cycles



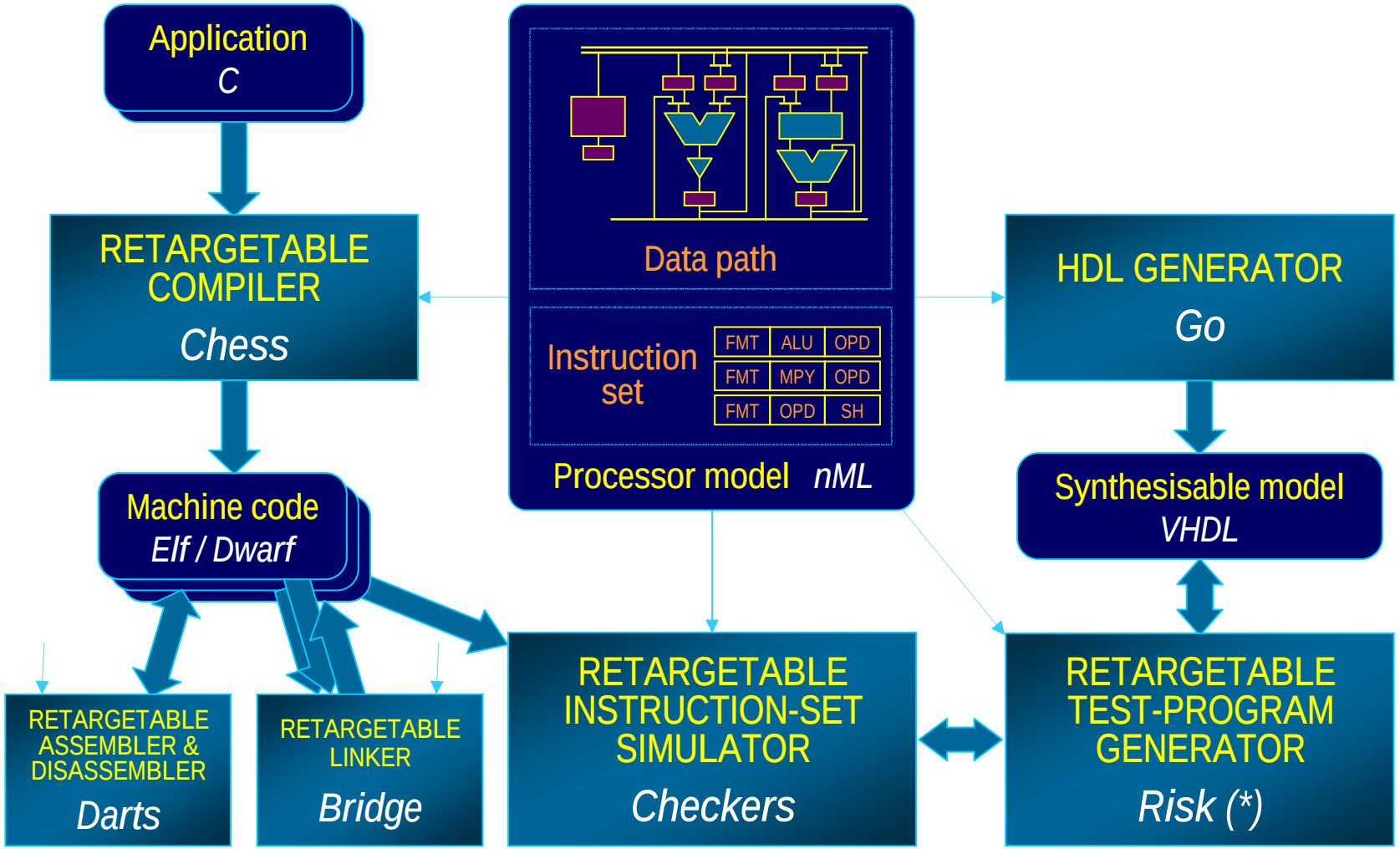


Processor architecture exploration & optimization (Philips)

- Processor Architecture exploration & optimization
  - Further optimization of audio DSP: required cycles, new instructions
  - Adding specific fixed point types and related functions for easier Software development supported by compiler
  - Improved DMA performance for better system integration
  - Study on JTAG based debug interface
  - Achieved better performances and power consumption (ex. MP3@1mWatt)
  - Cooperation with TCT using Chess and Checker toolsuite

- HW/SW Co-design flow based on SystemC
  - Using Aspects &YAPI-tools for system specification
  - Pilot case defined around CoolFlux DSP
  - Pipe-cleaned SystemC based co-design flow
  - Integrating CoolFlux DSP Instruction Set Simulator with SystemC in cooperation with TCT

Chess-Checkers from Target Compilers (TCT)



(*) Development planned in MESA, alpha version completed

Thank you !

To contact MESA :

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- **Global goals and organization**
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Maturity of outcomes : prototypes 2002

WP	Who	What
Prototypes exercized on a test-case		
1	IMEC	ATOMIUM Storage bandwidth optimization (SBO, MAA, ADOPTdemo done at DAC '2002)
2	EPUN	CoFluent Studio performance evaluation tool experimented
2	Philips	Æthereal: First prototype design and evaluation of Network-On-Chip router
2	ST	Method for debugging embedded SW
3	INRIA	C to C optimizer
3	Philips	COCOON automatic generation of DSP processors & their compilers
3	PolySpace	Run-time errors verifier for DSPs
4	MetaSymb	MetaSymbiose Logan.H hierarchical model checker
4	Philips	Property checking method
4	TIMA	Theosim: improvement of 2001 prototype for a VHDL subset

- A wide set of inter-operatable tools :
  - >10 prototypes
  - >20 exploitable tools

Maturity of outcomes : prototypes 2003

WP	Who	What
1	IMEC	Interface for task concurrency management
1	Philips	ASPECTS-2 System-level architecture exploration
2	Alcatel	HAL (Hardware Abstraction Layer) generator
2	Coware	PBD Platform Based Design
2	KUL	CRISP architecture
3	ARM	Dedicated DSP Data Engine tool OptimoDE
3	CAPS	XemSys Tuner code optimizer
3	TCT	RISK test programme generator
4	Bull/MetaSym.	Virtual Composer Platform
4	Philips	PDSL Portable Prototyping Platform (P4) extended with HW acceleration capabilities
4	Philips	Compiler for TRIMEDIA core

New 2003 !

Maturity of outcomes : ready for exploitation

2002

WP	Who	What
Market		
1&3	ARM	Basic pointer and class support integrated in the commercial (v3.1) A|RT. NB: A|RT will be embedded in ARM OptimoDE reprogrammable Data Engine compiler, to be marketed in 2004
Internal exploitation		
2	Philips	DTL: Product version for in-house use
4	MetaSymb.	LOGAN: new version of an industrial hierarchical model checker
3	ST	FlexCC2 infrastructure for automatic retargeting of SW

New 2003 !

WP	Who	What
Market		
2	Coware	N2C / SystemC
4	MetaSymb.	LOGAN hierarchical model checker V.3 PSL/Sugar
3	PolySpace	PolySpace Verifier, beta version
Internal exploitation		
	Philips	ERC SW mapping on architecture of standard processors
4	ST	Test-bench environment (Verisity) linked to emulation (Celaro, Mentor)